SiC JFET/P-MOSFET cascode for SSCB and inrush current limiter in 300V DC power systems

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***Abstract*—This work presents a solid-state distribution and protection switch based on the SiC JFET/P-MOSFET cascode structure. The concept is aimed for 300V applications, but it can be adapted easily to other voltages. Detailed circuit design and simulation is discussed, as well as the potential application in 300V bus voltage satellites.**

Keywords—SSCB, SiC JFET, P-MOSFET, cascode, current limiter, satellite, DC voltage

I. INTRODUCTION

Ubiquitous electronics (including computers, communications, and entertainment systems), LED lighting, and different electric vehicles are increasing the demand for DC power. Further, many renewable energy sources and energy storage systems either are DC natively or use a DC link in their power electronics interface. Also, when comparing with AC distribution, DC distribution does not suffer from synchronization issues and control is simpler since there are no reactive power and harmonic power. These, and other, reasons have triggered the use of DC distribution systems in many applications to improve the energy efficiency.

Protection in DC distribution is different from AC distribution. Higher short circuit currents with large di/dt and continuous DC arc ask for solid-state devices with faster switching speed, instead of traditional fuses and electromechanical overcurrent protection devices. In recent years, some solid-state overcurrent protection devices have been proposed for different DC distribution systems. Many examples can be found in literature review papers [1-2]. Most of them are in the extra low (ELV) and low voltage (LV) DC range 24V – 1500V.

Solid-state DC overcurrent protection devices have adopted different names depending on the characteristics and field of application. For instance, Solid-State Circuit Breakers (SSCBs) are protection apparatuses for current fault interruption, devised to open the power semiconductor as fast as possible once the current exceeds certain value. These devices should withstand with large fault currents and turn-off the protection switch in few microseconds. On the other hand, Solid-State Power Controllers (SSPCs) are devices that are usually found aeronautics and space applications. SSPCs are advanced protection devices that, in addition to overcurrent protection, also include inrush current control with current limitation during a pre-programmed trip-off time, remote on/off control, under and over voltage protection, and thermal protection. They are usually employed for end-user protection and limitation current does not exceed few tens of amps while trip-off time remains in the range of few miliseconds [3-4]. These devices can be also found as hot swap controllers and electronic fuses as integrated circuits for ELV ranges.

Since wide bandgap semiconductors, especially SiC, have already reached an important maturity level, SSCBs and SSPCs up to 400V for any application could benefit from the advantages of SiC technology (higher thermal conductivity, higher critical electric field, and higher intrinsic temperature). It allows higher current and power densities inside the devices, as well as lower losses and faster response. In particular, SiC JFET have been revealed very interesting for current limitation purposes, i.e. active mode operation.

Recent literature illustrates this situation with several examples. Normally-on SiC JFET based, 400V, nominal current up to 5A, with a turn-off current up to 200A, and with a current interruption time shorter than 800ns is reported in [5]. A SiC cascode based, 380V, 80A with a response time of 9.4us is described in [6]. Authors have also proposed a SiC cascode with an isolated photovoltaic driver, self-powered, 380V, 4.5A, fault current limiter, that has response time less than 600ns in [7].

A common issue in these cases regards to gate driving. Being the SiC JFET a normally-on device, it requires a control mean to properly start-up the different controlled loads. Commonly, to convert the SiC JFET into a normally-off device, an N-channel Si MOSFET is added in cascode configuration. The N-channel MOSFET requires a high-side driver. On the other hand, to simplify the gate driving issues, P-channel MOSFETs are widely used for SSPCs in the ELV range (<50V), but unfortunately, they are not suitable for higher voltages.

It is in this context that the P-channel MOSFET and the SiC JFET in cascode configuration can offer the following advantages:

- Simple gate driving circuit referred to the input voltage allows self-powering.

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- High voltage blocking and very low on-resistance (P-channel MOSFET is very low voltage $V_{DS\ max}$<30V)
- Ease of SiC JFET paralleling controlled by a single P-channel MOSFET allow power (i.e. current) scalability.
- Serialization of SiC JFET is possible with supercascode structures to increase voltage blocking capabilities [11].
- Low parasitic capacitances allow switching operation, which opens the door to different control schemes such as fully switching current limitation or hybrid linear-switching current limitation.

This composite power device has been recently explored for SSCB applications [8], and, by the authors, for SSPC in 100V satellite distribution systems [9].

The aim of this work is to investigate the utilization of such power devices at higher a voltage (up to 300V DC - 400V DC), and a higher current, with special emphasis in satellite power distribution and protection systems.

II. Composite power device: SiC JFET - PMOSFET cascode

The proposed composite power device, shown in figure 1, is a SiC JFET – PMOSFET cascode. Current measurement (shunt) resistor is optional as it could be placed in different positions, depending on the circuit topology. Zener (Z_1) and diode (D_1) clamp the maximum voltage for J_1 and M_1 protection.

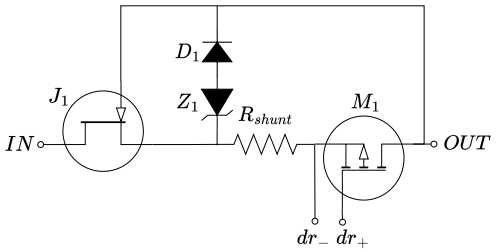

Fig. 1. SiC JFET - PMOSFET cascode, as proposed by the authors in [9].

As detailed in [9], the operation of such device is similar to the SiC JFET – N-MOSFET cascode. It has the three transistor regions: ohmic, cut-off and saturation. While the High-Side (HS) switch configuration operates in ohmic and cut-off, the Current Limiter (CL) function forces a constant current, thus operating J_1 and M_1 in saturation. It should be noted, that M_1 always blocks a restricted voltage, the J_1 pinch-off voltage, $|V_P(J_1)| < |V(Z_1)+V(D_1)|$, hence the most stressed device is J_1. In other words, to increase the current limitation performances of the device, J_1 should be carefully sized.

To increase the current limitation setpoint and trip-off time (defined as the time that the device operates in current limitation before turns off), a simple approach is to consider paralleled SiC JFET transistors controlled by a single P-MOSFET, as illustrated in figure 2.

Obviously, combinations of paralleled composite power devices increase the number of potential applications. As an example, this work proposes a SSCB with resistor-assisted inrush current control and active current limitation for load faults, as represented in figure 3. This approach allows large capacitor charging avoiding the losses in the power semiconductors, decoupling the design of the inrush current switch and the load fault current limiter.

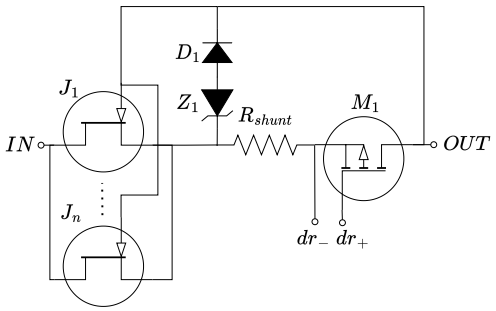

Fig. 2. Paralleled SiC JFET – single PMOSFET cascode.

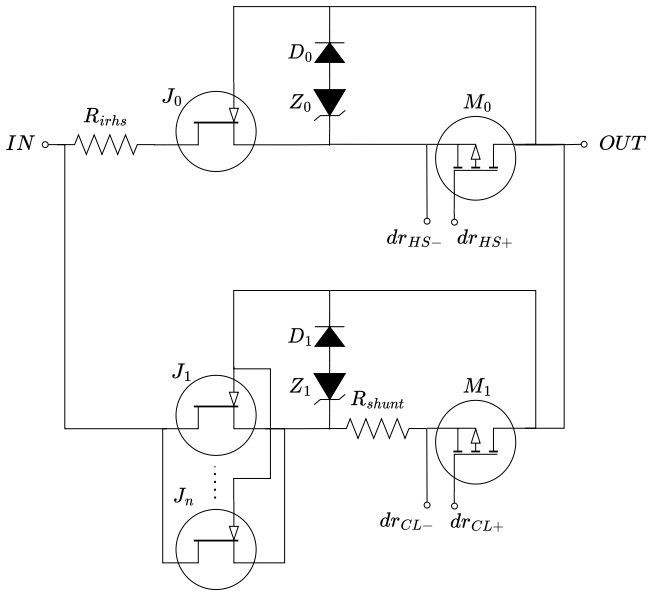

Fig. 3. Proposed composite power switch for SSCB with active current limitation and high-side switch with resistor-assisted inrush current limiter.

III. SSCB with active current limitation and resistor-assisted inrush current control

The block diagram of the proposed distribution circuit is shown in figure 4. The two switches can be designed as independent functions.

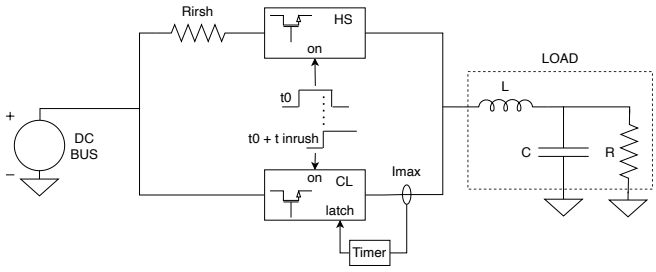

Fig. 4. Block diagram of the proposed SSCB.

The HS circuit is designed as follows. The ohmic value of the external inrush resistor (R_{irsh}) for the inrush control is given by the bus voltage divided by the desired maximum inrush current. Assuming that the reactive part of the load circuit is dominated by the capacitive part, the inrush time constant is simply obtained by the multiplication of the inrush

resistor and the capacitance. The inrush time (t_{irsh}) is then given by three times the time constant. Thus, t_{irsh} is the minimum required to activate the active current limitation switch (CL). Dividing the capacitor stored energy by the inrush time constant, an initial guess of the R_{irsh} wattage is found. Using the manufacturer datasheet and the guidance for power rating in single pulse operation, the final resistor wattage is determined.

The CL circuit is designed as follows. First, the load determines the nominal current (I_{nom}) and the limitation current, $I_{lmt}=1.1I_{nom}$. Limitation current determines shunt resistor value (R_{shunt}), which should be selected to have a voltage drop around 100mV to optimize the current monitor performance. The selection and number of paralleled SiC JFET, if required, and P-MOSFET are driven by the limitation current from the manufacturer datasheet information. SiC JFET voltage requirements is simply given by the bus voltage and P-MOSFET voltage requirements by the SiC JFET pinch-off voltage. Finally, the trip-off time is given by the SiC JFET and P-MOSFET transistor SOA. In a hard short-circuit at the output of the SSCB, the SiC JFET will block the input voltage while will carry the limitation current, $P_{JFET}=V_{in}\cdot I_{lmt}$. SOA information provides the maximum power allowed per unit time, which finally determines the trip-off time.

A design example is given next. The initial parameters are, V_{in}=300V, I_{nom}=10A and C=500µF.

$$R_{shunt}=\frac{100mV}{1.1I_{nom}}\approx 10m\Omega \tag{1}$$

$$P_{shunt}=\frac{(100mV)^2}{10m\Omega}=1W \tag{2}$$

$$I_{PMOS\,\max rating}=I_{JFET\,\max rating}=\frac{1.1I_{nom}}{0.2}=55A \tag{3}$$

$$R_{irsh}=\frac{V_{in}}{15A}=20\Omega \tag{4}$$

$$t_{irsh}=3\cdot C\cdot 20\Omega=30ms \tag{5}$$

$$P_{irsh}=\frac{V_{in}^2\cdot 30ms}{6\cdot 20}=22.5W \tag{6}$$

IV. Circuit Design

The key part of the CL switch is the current limiter circuit. Several ways to implement it are possible. A current sense amplifier can be used to measure the voltage drop on the shunt resistor and a second opamp amplifying stage could drive the P-MOSFET. However, this solution must consider the large common-mode voltage present in the shunt resistor, as well as the additional auxiliar power supplies required for the amplifiers. A simple and discrete solution for the current limiter is shown in figure 5.

This current limiter works on balancing the voltage drop in R_{shunt} and R_{Iadj}. If $V(R_{shunt})$ < $V(R_{Iadj})$, Q_{1a} blocks the reference voltage and M_1 turns on. When $V(R_{shunt})=V(R_{Iadj})$, a negative feedback loop is created and Q_{1a} adjusts the required voltage to drive M_1. Current limitation is adjusted by (7-8).

$$I_{LIM}=\frac{I_{bias}R_{Iadj}}{R_{shunt}} \tag{7}$$

$$I_{bias}=\frac{V_{ref}-2V_{BE(on)}}{R_{bias}} \tag{8}$$

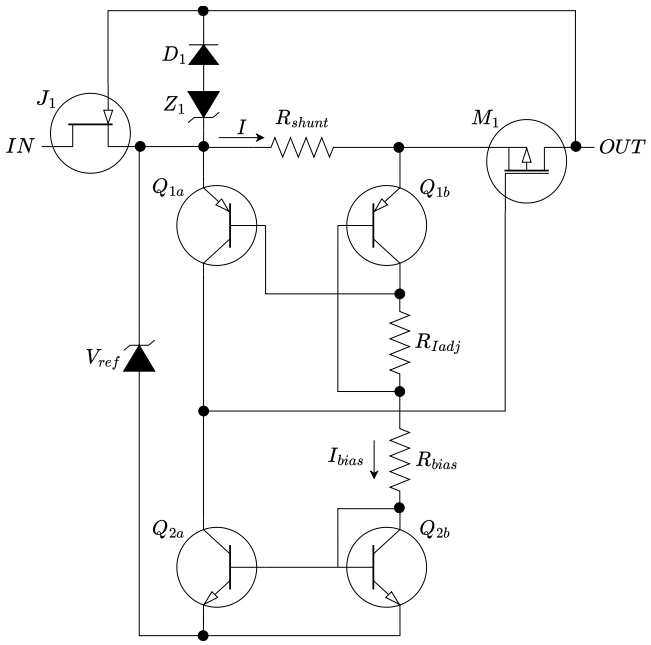

Fig. 5. Current limiter circuit for the proposed SSCB.

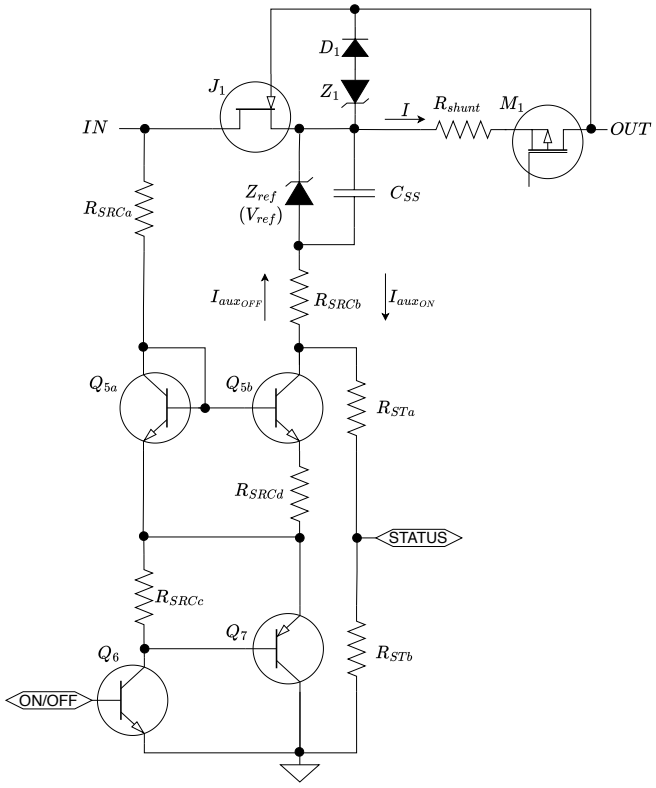

Fig. 6. Auxiliary bias circuit for the proposed SSCB.

The HS switch can be designed following the approaches of the discrete low-voltage load switches [10]. However, a more elaborated approach is shown in figure 6. This circuit sets the reference voltage (V_{ref}) to drive the P-MOSFET and the current limiter circuit, when command signal (on/off) is on, but it also drives the Z_{ref} in forward conditions and clamps the $V_{GS}(J_1)$=-(V(Z_1)+0.7V) to force the off-state of M_1 and J_1, when the command signal (on/off) is off.

Timer and latching circuits are shown in figure 7. These are devised to vary the trip-off time depending on the severity of the fault. The longest trip-off time occurs when load overcurrent fault is close to the limitation current, while the shortest trip-off time happens for hard overcurrent events. Maximum trip-off time is dominated by P-MOSFET SOA, while minimum trip-off time is defined by the SiC JFET SOA. The timing capacitor is charged by the constant current source I_{TMR2}, which is mirrored from I_{TMR1}. R_{TMR3} limits the maximum trip-off time when the overload current approaches the limitation current.

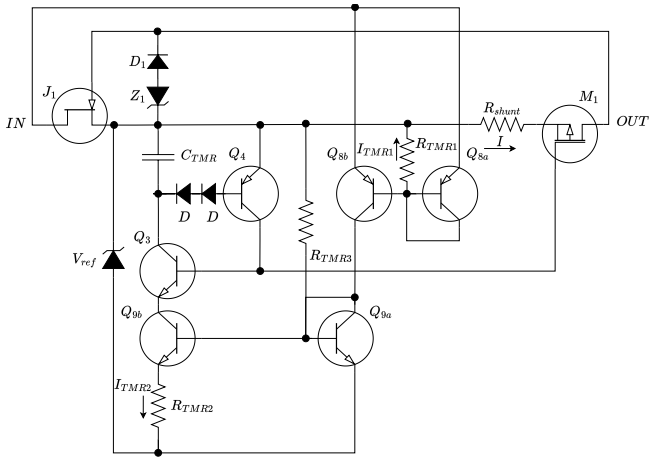

Fig. 7. Timer and latching circuit of the proposed SSCB.

V. SSCB TRANSISTORS SELECTION

For the CL switch, SiC JFET UJN1205K (1200V/23A/45mΩ) has been selected. To meet the current requirements in nominal, steady-state on conditions, $I_{JFET\ max\ rating}$=55A (3), three paralleled devices are required. Assuming an equal current sharing between devices, on-losses are approximately 1W per device. Considering SOA specifications, minimum trip-off time 300us is selected. The P-MOSFET is a SQD50P03-07 (30V/50A/7mΩ) that dissipates less 1W at nominal current. The maximum trip-off time following its SOA specifications has been defined to 5ms.

The HS switch transistor selection is driven by the maximum energy dissipated during the inrush current. The output capacitor energy is 22.5J, which is charged in 30ms. The number of paralleled SiC JFET required becomes impractical to perform active current limitation, so an additional external resistor is added. Resistor value has been selected to be 20%-30% higher than the limitation current. Most of the inrush energy is dissipated by the resistor, so a single SiC JFET UJN1205K (1200V/23A/45mΩ) is required. The P-MOSFET SQD50P03-07 (30V/50A/7mΩ) is also selected.

External power resistor should be selected for energy overload capability, as it corresponds during a short single pulse event. Wirewound power resistors are suitable for this application, two paralleled W24 47Ω from TT electronics are selected.

An RC damping network (1µF-4.7Ω) connected at the output helps to reduce di/dt of the SiC JFET during the fault events. This reduces maximum V_{DS} voltage in the SiC JFET.

VI. SSCB SIMULATION

The proposed concept has been fully modelled in LTspice. Inductance harness at input (15uH) and output (15uH) are considered, soft overload is 11.2A and hard overload is 118A.

A. Inrush current

Figure 8 shows the output voltage (top), the CL switch current (middle) and the HS switch (bottom) during the initial output capacitor charging. It is clearly observed that inrush current is provided by the HS switch which is limited by the external resistors. The final charge is completed by the CL switch until it reaches the load current, 0.5A.

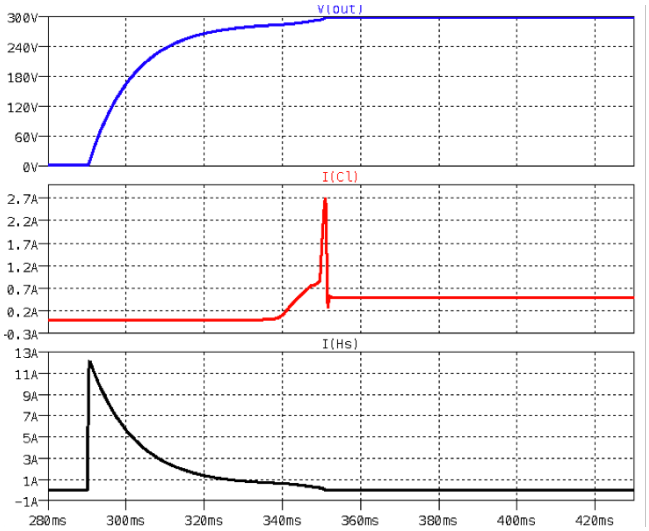

Fig. 8. Inrush current. Output voltage (top), CL switch current (middle), HS switch (bottom).

Figure 9 shows the power waveforms of the main elements during the inrush interval. It is observed that external resistors are the most dissipative elements, keeping low dissipation in the power transistors.

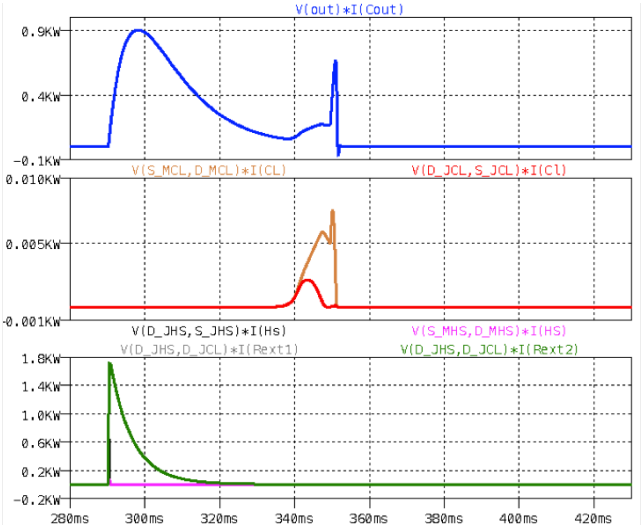

Fig. 9. Inrush current. Capacitor charging power (top), CL-JFET switch power (middle-red), CL-PMOS switch power (middle-orange), HS-JFET switch power (bottom-black), HS-PMOS switch power (bottom-pink), HS switch Rext1 power (bottom-grey), HS switch Rext2 power (bottom-green).

B. *Hard overload*

The hard overload, 118A current load, produces the interruption of the current in 210us approximately. The SiC JFET voltage is limited to 700V due to the RC snubber (1µF-4.7Ω). Parallel MOV on the SiC JFET could be used for additional protection. It is observed that the composite switch reacts very fast to go into limitation before the fault current goes very large. In addition, the di/dt during the turn-off performs softly to avoid non desired turn-on. Finally, as the SSCB reacts fast, the output capacitor has not discharged and the SiC JFET power losses are minimal.

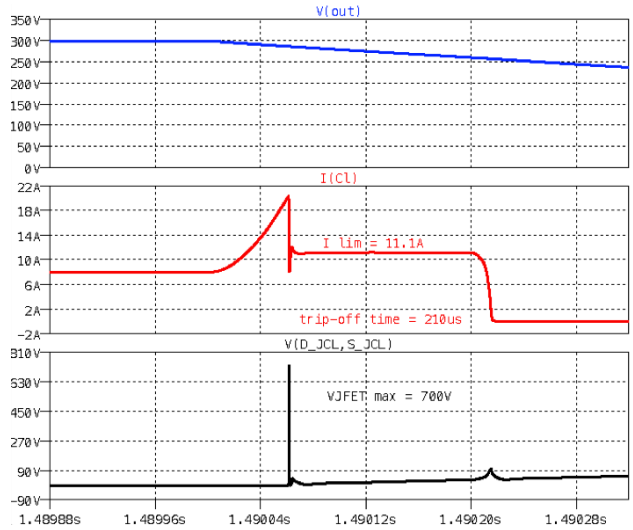

Fig. 10. Hard overload. Output voltage (top), CL switch current (middle), CL-JFET switch power (bottom).

C. *Soft overload*

The soft overload, 11.4A current load, is interrupted in 4.6ms, since power dissipation in power semiconductors is less critical than in the previous case and gives the opportunity to the system to recover from unexpected load current demand. In this case, the effect of the di/dt in the JFET voltage is not observed.

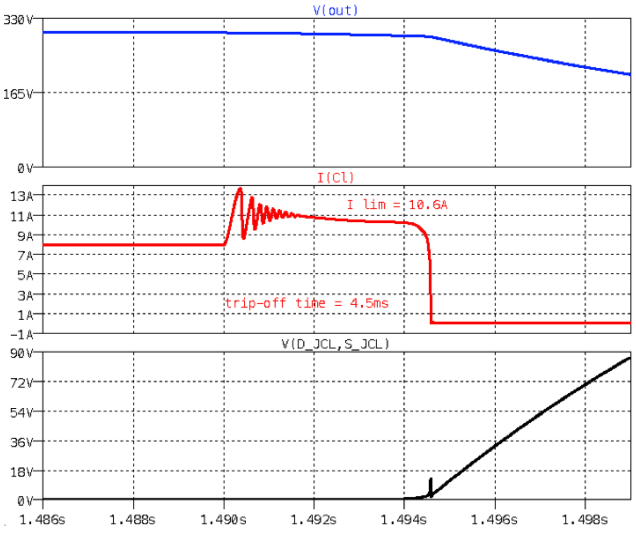

Fig. 11. Soft overload. Output voltage (top), CL switch current (middle), CL-JFET switch power (bottom).

VII. Discussion: Application to Satellites

High-power satellites employ 100V-120V bus voltage regulated distribution, but 300V-400V is becoming an interesting option for larger power satellites. It is apparent that distribution switches are key for adopting 300V bus voltage.

Low power and medium power satellites usually distribute 28V and 50V, employing P-MOSFET as the main power semiconductor for implementing the current limited, switchable distribution switches. These devices are commonly referred as Latching Current Limiters (LCLs) in European industry and agencies. As described in the European Space Agency (ESA) standards [12], [13] and guidelines [14], LCLs are classified into classes depending on the maximum current that they can carry, from 1A to 10A, however, they are only defined for 28V and 50V.

The extrapolation of the values from 28V to 300V bus has deep implications in terms of power dissipation. Keeping the same current and trip-off time limits [12], the values for 300V LCLs are summarized in table I.

TABLE I. Hyphotetical 300V LCLs specifications

Class	1	2	3	4	5	6	8	10
Ilim min(A)	1.1	2.2	3.3	4.4	5.5	6.6	8.8	11
Ilim max(A)	1.4	2.8	4.2	5.6	7	8.4	11.2	14
t_trip min(ms)	10	10	6	6	4	2	2	1.5
t_trip max(ms)	20	20	12	12	8	4	4	3
Cload max(uF)	25	51	46	61	51	31	41	38

From these values, it can be observed that maximum load capacitances have been largely reduced compared to 28V bus [12], but the inrush energy involved in the load capacitor charging and the energy dissipated in the limiting element during an ideal short-circuit still are large, see table II.

TABLE II. Hyphotetical 300V LCLs energy

Class	1	2	3	4	5	6	8	10
E_Cload (J)	1.1	2.3	2.1	2.7	2.3	1.4	1.8	1.7
E_SC max (J)	8.4	17	15	20	17	10	13	13

In order to provide a solution for increasing the load capacitance by a factor ten and keep low energy dissipation in case of overload, the protection device could be split in two parts as proposed in this work. A HS switch with external resistor is designed to provide inrush energy demanded by the load capacitor. In case of overloads, the CL switch limits the current, but it also adjusts the trip-off time depending on the severity of the fault.

VIII. Conclusion

This work presents an approach for a SSCB with selectable current limiting capabilities, self-adjustable trip-off time and additional resistor-assisted inrush current limiter. The solution is based on a novel SiC JFET/P-MOSFET structure that has the advantages of the P-MOSFET driving and increases the high blocking voltage capabilities and low conduction losses. The concept has been applied to a distribution and protection switch on hypothetical 300V satellite bus, although it can be applied to other DC distribution systems and voltages.

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