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Sequential Switching Shunt Regulator Parallel Power Processing Control for High Capacitance Solar Arrays

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Abstract: This paper presents a new control strategy for reducing the switching losses produced by the use of high parasitic capacitance solar arrays in the sequential switching shunt regulator. Instead of dividing the solar array into equal sections, the proposed strategy is based on two different sections types, low-capacitance and high-capacitance ones. In order to reduce the switching losses and to maintain the original closed-loop response, a novel parallel power processing control strategy is implemented. With this new technique the low-capacitance sections are the only ones that switch at high frequency to regulate the bus while the high-capacitance sections are only connected or disconnected under high load power changes. In addition, the control closed loop delay associated to the time needed to charge the parasitic capacitance has been modelled and a controller modification is proposed to reduce AC performance degradation.

Keywords: solar array regulator; sequential switch shunt regulator; solar array parasitic capacitance

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1. Introduction

Currently, in European high-power telecommunication satellites, the regulated power bus is the most used power bus architecture [1]. In this architecture, the main bus voltage is always regulated by the main error amplifier (*MEA*), which controls all the power converters: the solar array regulator (*SAR*), the battery charge regulator (*BCR*) and the battery discharge regulator (*BDR*), see Figure 1.

To date, the most used *SAR* subsystem is the sequential switching shunt regulator (S^3R) due to its high efficiency, low mass, simplicity and high reliability [2,3]. In Figure 2, a simplified S^3R schematic diagram is presented; as can be seen, the solar array is divided into n equal sections and each one is connected to a shunt regulator so the section can be short-circuited or connected to the bus. The *MEA* is in charge of controlling which sections are connected directly to the bus, which sections are short-circuited and which is the only section that switches to regulate the bus voltage.

Currently, due to the use of multijunction solar arrays, the solar array parasitic capacitance (C_{SA}) has increased considerably, complicating the S^3R design. The main reason for the C_{SA} increase is the use of triple and quadruple junction solar cells. Current quadruple junction technology presents a very high efficiency, up to 32% of what is directly reflected in a solar array mass and volume reduction. However, it also shows a higher parasitic capacitance that can be up to five times larger than silicon technology for the same voltage and power [4–7]. As reported in [8], the impact of a higher C_{SA} on the S^3R can be summarized as follows:

- The requirement to use an active current limiter [3,9] to avoid the current spikes produced by the discharge of the C_{SA} at shunt–transistor turn on. When one solar array section is connected to the bus, the C_{SA} is charged to the bus voltage. That energy is dissipated in the shunt transistor when it turns on. The requirement to use an active current limiter has a major drawback because the shunt transistor switching time increases drastically, and this results in an increase of the switching power losses.

- Increase of the dump turn-on delay penalizing the *DC* characteristic (output voltage ripple) and the *AC* characteristics (regulator bandwidth and output impedance).

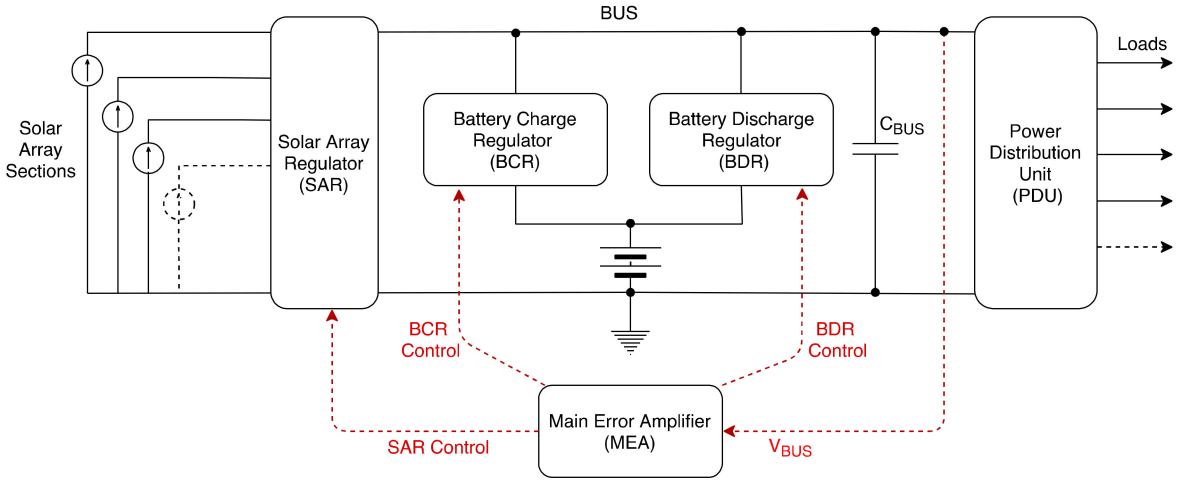

Figure 1. Regulated power bus architecture.

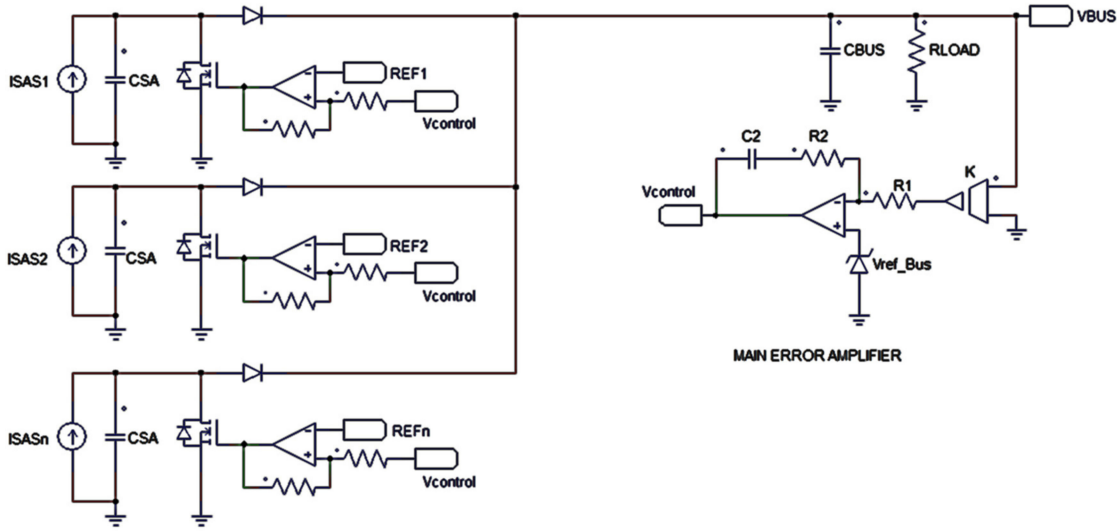

Figure 2. Sequential switching shunt regulator (S^3R) simplified schematic.

A possible solution to these problems is the use of smaller solar array sections or/and to increase the bus capacitance (C_{BUS}). The benefit of having smaller sections is the reduction of the C_{SA}, which combined with an increase of the C_{BUS}, reduces the switching frequency and improves the *AC* characteristics of the system. These solutions also have a constraint at system level; a high number of sections or a higher C_{BUS} penalize the system in terms of mass and volume. Another proposed solution to reduce the switching frequency is the use of nesting on the S^3R cells [10], but with the penalty of making the transconductance gain depend on the regulator operating point and complicating the control loop design.

The focus of this paper is to present a novel solution to minimize the problems described above. In the proposed solution, the traditional S^3R topology is used, but instead of dividing the complete solar array into equal sections, two types of sections will be used. The solar array will be divided into two types of sections: low and high current solar array sections. A new parallel power processing strategy has been developed, so the small sections are the only ones that switch to regulate the bus, achieving lower switching power losses. In addition, the use of small sections to regulate the bus reduces the current ripple

on the bus capacitor. The high-power sections are only connected or disconnected during high load power changes.

This topology, but with a different control method, has already been used in the Agile Satellite [10] and proposed with a hybrid analog–digital control in [11]. In the Agile Satellite *SAR*, the low-power sections hysteric windows control references are located inside the high-power sections ones. This control method produces a regulator that does not have a constant transconductance gain, the transconductance gain depends on the operating point of the regulator, making the modeling and design of the control loop difficult. The modeling and design of the hybrid analog–digital control presented in [11] is quite difficult due to its digital part. The novelty of the control method presented in this paper is that the regulator has exactly the same first order response as the traditional S^3R, with a constant conductance, independent of the regulator working point, and the control loop implanted is entirely analog.

This new topology is modeled, simulated and implemented with satisfactory results, reducing the power losses and facilitating the thermal design. On the other hand, the sections turn-on delay due to the C_{sa} is mathematically modeled so that the impact in the *AC* characteristics of the regulator can be represented and analyzed. Using the delay model, a new control loop design is suggested to reduce the impact of the delay. This control loop is also modeled and simulated, thus improving the *AC* behavior of the regulator.

2. Proposed S^3R Control Method

The traditional S^3R topology is used, but the solar array is divided into two types of sections: low current solar array sections (*sas*) with low parasitic capacitance (C_{sa}), and high current solar array sections (*SAS*) with high parasitic capacitance (C_{SA}). The control strategy is modified so the small sections are the only ones that switch to regulate the bus, producing low switching power losses. The modification consists in a new distribution of the hysteric windows control references of all the sections and the inclusion of an analog subtractor in the low C_{SA} sections *MEA* control loop; the proposed solar array regulator is depicted in Figure 3.

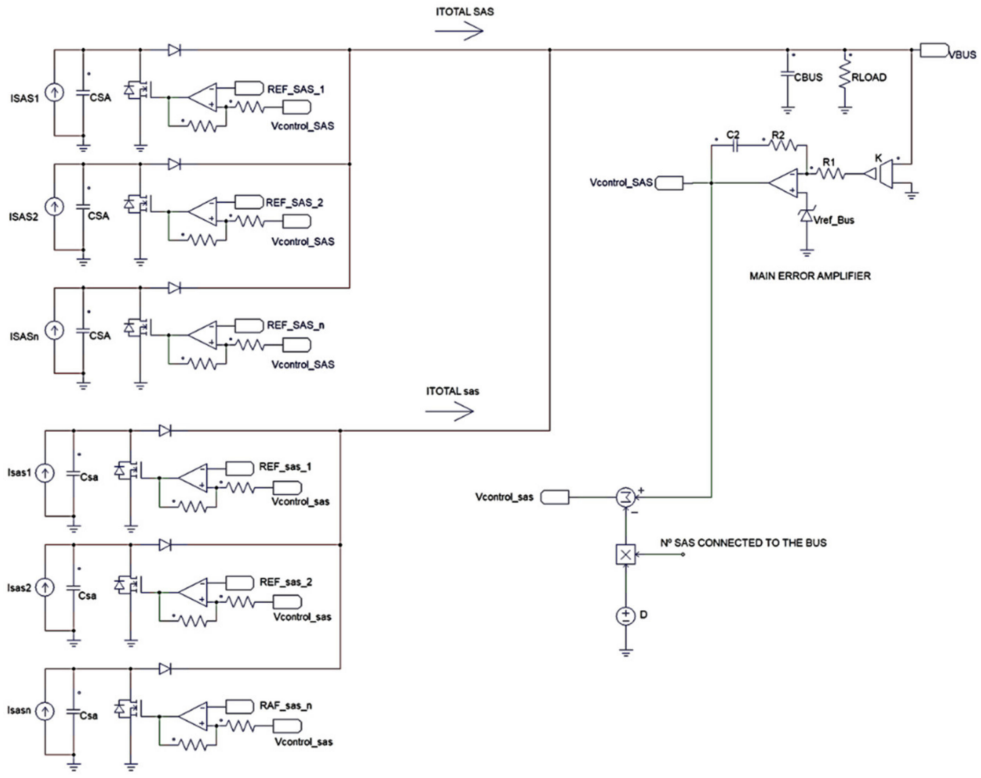

Figure 3. Proposed solar array regulator.

The number of low-power solar array (N_{sas}) sections needed is given by the division of the current of a high-power section (I_{SAS}) by the current of a low-power section (I_{sas}), adding one more section for redundant purposes, see Equation (1).

$$N_{sas} = I_{SAS} \ / \ I_{sas} + 1 \tag{1}$$

For a given regulator conductance (G), the low-power sections hysteric comparator window references have a width (v_{hl}) defined by Equation (2) and distributed as is shown in Figure 4.

$$v_{hl} = I_{sas} \ / \ G \tag{2}$$

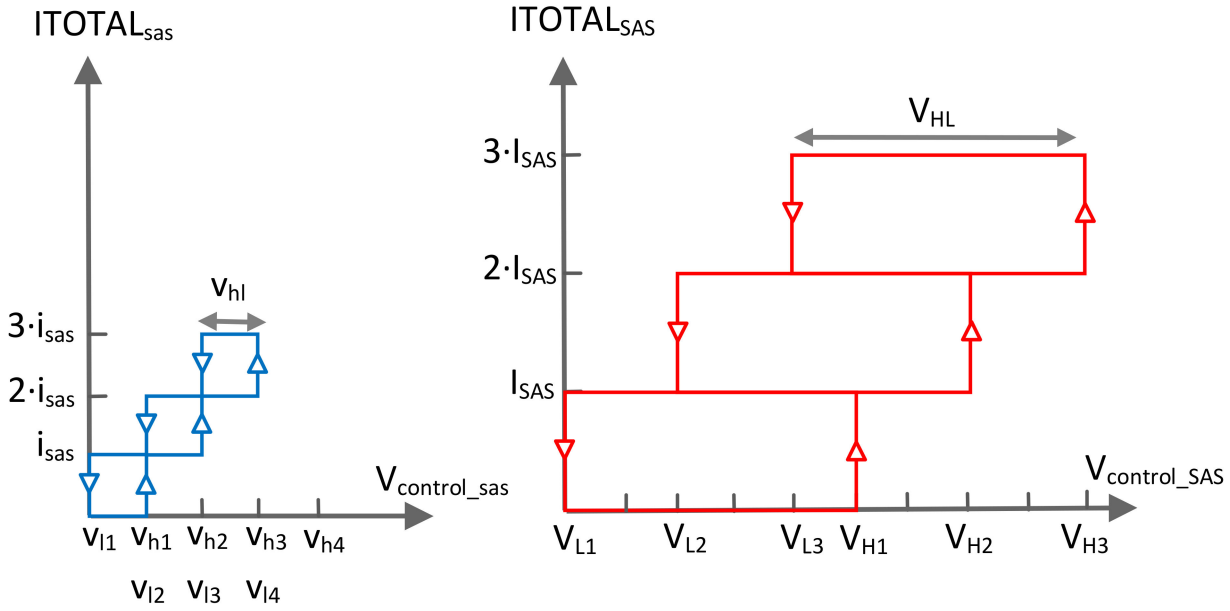

Figure 4. Hysteretic comparator window references: low-power sections (blue) and high-power sections (red).

In order to maintain a constant regulator conductance, and that the low-power sections are the only ones that switch to regulate the bus, the high-power sections hysteric comparator window references have to be distributed as shown in Figure 4. The width of these reference windows (V_{HL}) is defined by Equation (3).

$$V_{HL} = V_{hl} \cdot (N_{sas} + I_{SAS} \ / \ I_{sas}) \tag{3}$$

The high-power section n hysteric window lower limit (V_{Ln}) is given by Equation (4), where v_{l1} is the first low-power section lower limit reference.

$$V_{Ln} = v_{l1} + V_{hl} \cdot (n - 1) \cdot I_{SAS} \ / \ I_{sas} \tag{4}$$

A new control signal (V_{ERROR_sas}) is needed to control the low-power sections, see Figure 3. The substractor, included in the low-power sections control loop, subtracts a voltage (D) to the original *MEA* control signal (V_{ERROR}) proportional to the high-power sections connected to the bus (N_{SAS_ON}), see Equations (5) and (6).

$$V_{ERROR\_sas} = V_{ERROR} - D \cdot N_{SAS\_ON} \tag{5}$$

$$D = I_{SAS} \ / \ G \tag{6}$$

Figure 5 shows a waveform example of the new control operation. The different situations shown are detailed next.

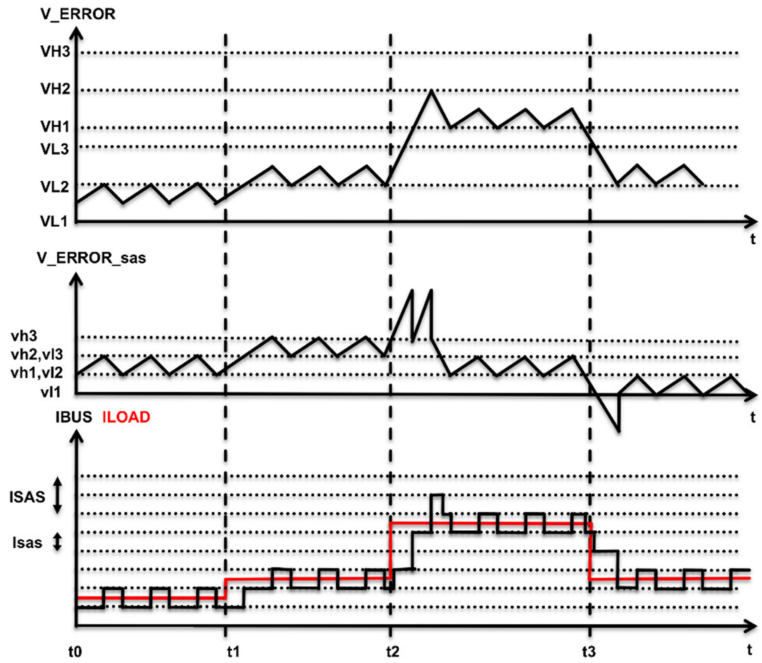

Figure 5. Typical regulator waveforms.

- From t0 to t1 (steady state response): In this state, the low-power Section 2 switches to regulate the bus voltage, while all the high-power sections are fully off. The total load-averaged current is given by Equation (7).

$$I_{LOAD} = I_{sas1} + <I_{sas2}> \tag{7}$$

- From t1 to t2 (small load perturbation): At t1, a load current step occurs. V_{ERROR} and V_{ERROR_sas} increase switching on the upper low-power current sections until the current balance is reached. In this case, the compensation is achieved with the third low-power section. Since the V_{ERROR} signal does not cross the V_{H1} threshold, the high-power sections are not connected. This is the classical S^3R response. In this case, the total load-averaged current is given by Equation (8).

$$I_{LOAD} = I_{sas1} + I_{sas2} + <I_{sas3}> \tag{8}$$

- From t2 to t3 (large load perturbation): At t2, a large load current step occurs. Now the low-power sections remaining current is insufficient to compensate the load change. After switching on all the low-power sections, V_{ERROR} increases until it crosses the V_{H1} threshold; at this moment the high-power Section 1 is switched on and a constant voltage is subtracted to V_{ERROR} to generate V_{ERROR_sas}. The compensation is not yet achieved, so V_{ERROR} increases until it crosses the V_{H2} threshold, at this moment the high-power Section 2 is switched on and the voltage subtracted to V_{ERROR} to generate V_{ERROR_sas} is doubled, see Equation (9). Now the balance between bus and load currents becomes positive so the control voltage decreases, and the system enters in the small power sections regulation zone. The fine current balance is achieved with the second small power section. The total load-averaged current is given by Equation (10).

$$V_{ERROR\_sas} = V_{ERROR} - 2 \cdot D \tag{9}$$

$$I_{LOAD} = I_{sas1} + <I_{sas2}> + I_{SAS1} + I_{SAS2} \tag{10}$$

- From t3 to t4 (large load perturbation): At t3, a large load current step occurs. All the low-power sections are switched off, but this is insufficient to compensate the load change. After switching off all of the low-power sections, V_{ERROR} still decreases until

it crosses the V_{L2} threshold; at this moment the high-power Section 2 is switched off and the voltage subtracted to V_{ERROR} to generate V_{ERROR_SAS} is given by Equation (11). Now the balance between the bus and load currents becomes negative so the control signals increase and the system enters into the small power sections regulation zone. The fine current balance is achieved with the first small power section. The total load-averaged current is given by Equation (12).

$$V_{ERROR\_sas} = V_{ERROR} - D \tag{11}$$

$$I_{LOAD} = <I_{sas1}> + I_{SAS1} \tag{12}$$

3. Shunt Transistor Turn-On Delay Modeling

The *AC* characteristics of the regulator are not improved with the new control proposed in the previous section. The AC characteristics with the new control are exactly the same as the ones in the classical S^3R. The shunt transistor turn-on delay (τ_{delay}) is not improved because the relationship between the parasitic capacitance and the current for each section is constant, see Equation (13).

$$\tau_{delay} = \frac{V_{BUS} \cdot C_{SAS}}{I_{SAS}} = \frac{V_{BUS} \cdot C_{sas}}{I_{sas}} \tag{13}$$

The parasitic capacitance effect can be modeled as a delay in the control signal. As suggested in [3], to model the delay, the Padé second order approximation is used, see Equation (14).

$$\tau_{delay}(s) = \frac{s^2 - \frac{6s}{\tau_{delay}} + \frac{12}{\tau_{delay}{}^2}}{s^2 + \frac{6s}{\tau_{delay}} + \frac{12}{\tau_{delay}{}^2}} \tag{14}$$

This delay is placed in series in the control loop, producing degradation in the regulator gain margin (*GM*), phase margin (*PM*) and output impedance (Z_O). With the delay, the regulator loop gain (*TBUS*) is given by Equation (15).

$$TBUS(S) = k \cdot G \cdot \frac{1 + R_2 \cdot C_2 \cdot s}{R_1 \cdot C_2 \cdot s} \cdot \frac{R_{LOAD}}{1 + R_{LOAD} \cdot C_{BUS} \cdot s} \cdot \tau_{delay}(s) \tag{15}$$

To accomplish the European Space Agency (*ESA*) ECSS-E-20C standard, the *PM* should be at least 50° and the *GM* 6 dB for worst case end-of-life conditions. A practical design principle is to assure a 60° *PM* and 10 dB *GM* for begin-of-life conditions. Circuit simulations show that the maximum crossover frequency (w_{cbus}) (Equation (16)) to assure a 60° *PM* and 10 dB *GM* is given by Equation (17).

$$\omega_{cbus} = \frac{k \cdot G \cdot R_2}{R_1 \cdot C_{BUS}} \tag{16}$$

$$\omega_{cbus} \leq 0.14 \cdot \omega_{pdelay} = 0.14 \cdot \frac{\sqrt{12}}{\tau_{delay}} \tag{17}$$

The impact of the delay in the regulator output impedance (Z_O) is shown in Equation (18).

$$Z_O(S) = \frac{R_1 \cdot C_2 \cdot s}{R_1 \cdot C_2 \cdot C_{BUS} \cdot s^2 + R_2 \cdot C_2 \cdot k \cdot G \cdot \tau_{delay}(s) \cdot s + k \cdot G \cdot \tau_{delay}(s)} \tag{18}$$

If the phase margin is greater than 60°, the maximum value of the output impedance (Z_{Omax}) is not affected by the delay and is given by Equation (19).

$$Z_{Omax} = \frac{R_1}{R_2 \cdot G \cdot k} \tag{19}$$

To minimize the effects produced by the parasitic capacitance, the addition of a lead–lag network in the regulator control loop is proposed, improving the *AC* characteristics of the system. This lead–lag network is located in series with the main error amplifier (*MEA*) and only in the *SAR* control loop. The proposed lead–lag network is shown in Figure 6.

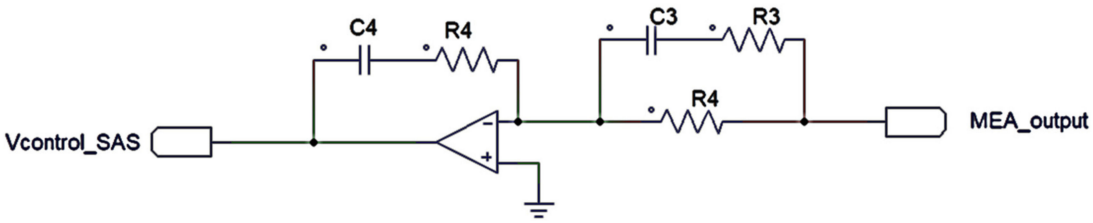

Figure 6. Lead–lag network.

This network adds one zero and two poles in *TBUS* function (15); simulations show that the best position to place the zero is given by Equation (20); one pole is placed one decade over the poles added by the delay, Equation (21), and the other one is placed at high frequency.

$$\omega_{zero\_lead\_lag} = \frac{1}{R_4 \cdot C_3} = 1.2 \cdot \frac{\sqrt{12}}{\tau_{delay}} \tag{20}$$

$$\omega_{pole1\_lead\_lag} = \frac{1}{R_3 \cdot C_3} = 10 \cdot \omega_{pdelay} = 10 \cdot \frac{\sqrt{12}}{\tau_{delay}} \tag{21}$$

The consequence of adding the lead–lag network is that the maximum crossover frequency (to accomplish with a 60° *PM*) is given by Equation (22), achieving an increase of 15%, directly proportional to a reduction in the bus capacitor capacitance.

$$\omega_{cbus} \leq 0.165 \cdot \omega_{pdelay} = 0.165 \cdot \frac{\sqrt{12}}{\tau_{delay}} \tag{22}$$

4. Simulation Results

To test the behavior of the proposed new control scheme, a system design for a 4.5 kW satellite is proposed. The bus voltage, voltage ripple and maximum output impedance are calculated using the guidelines provided in the ECSS-E-20C *ESA* standard. In addition, a 60° *PM* and 10 dB *GM* for begin-of-life conditions are imposed in order to assure the accomplishment of the standard *PM* and *GM* for worst case end-of-life conditions.

The parasitic capacitance used for the simulations is based on the Azurspace 3G28 solar cell capacitance studies presented in [12]; a 2.25 µF capacitance per cell (0.5 A *Isc*, 2.5 V *Voc*) is proposed in this paper. For a 50 V bus, twenty cells in series are needed in each solar array section so the resultant parasitic capacitance is 225 nF/A. This value is increased to 300 nF/A for derating considerations. The proposed system specifications are listed in Table 1.

Table 1. System specifications.

System Specifications	
Power	4500 W
C_{sa}	0.3 µF/A
Bus voltage (V_{BUS})	50 V
Bus voltage ripple (ΔV_{BUS})	<1% V_{BUS}
Maximum output impedance ($Z_{O\,max}$)	11.1 mΩ
Control loop gain margin	≥10 dB
Control loop phase margin	≥60°

The system is designed based on the conductance control method design guidelines presented in [13] and the proposed Equations (20)–(22). In Table 2, the final system parameters are listed.

Table 2. Simulated system parameters.

System Specifications	
Number of high-power solar array sections (*SAS*)	10 (7 A/section)
Number of low-power solar array sections (*sas*)	6 (3.5 A/section)
Bus capacitance	2.76 mF
G	7 A/V
K	0.1
R1	1 kΩ
R2	145 kΩ
C2	5 nF
R3	100 Ω
C3	3.7 nF
R4	1 kΩ
C4	3 pF

The proposed design was simulated using *PSIM* simulator from Powersim Inc. In Figure 7, the simulation results are shown. In the top of the figure, it can be seen in red the bus voltage and in blue the output of linear model of the regulator. In the middle of the figure are shown the different currents in the system; in pink the load current is shown; it can be seen that a 45 A load step is simulated. The high-power sections bus current (*ISAS*) is depicted in red, the low-power section bus current (*Isas*) is in blue and the total bus current (*IBUS*) is in green. As expected, the low-power sections are always the ones that switch to regulate the *BUS* voltage. In the figure bottom, the two error signals are shown; the high-power sections error signal (*MEA*) can be seen in red and the low-power section error signal (*Verror_sas*) is shown in blue. It can be appreciated that each time a high-power section is connected to the bus, a constant voltage is subtracted to *Verror_sas*.

In Figure 8, the simulation of the control loop response (*TBUS*) is shown. In blue is shown the response without the lead–lag network and without considering the delay ($PM = 87.9°$). In green is shown the classical response, but considering the delay produced by the C_{SA}, the *PM* is degraded to 55.3°. In red is shown the response using the lead–lag network and considering the delay, the *PM* is improved to 62.1°.

In Figure 9, the regulator-simulated output impedance (*Zo*) simulation is shown. The dashed line shows the output impedance mask to accomplish the *ESA* standard, in blue is shown the response without the lead–lag network and without taking into account the delay. In green is shown the classical response, but taking into account the delay produced by the C_{SA}. In red is shown the response using the lead–lag network and taking into account the delay. In all of the cases, the standard is accomplished, but the addition of lead–lag network improves the output impedance.

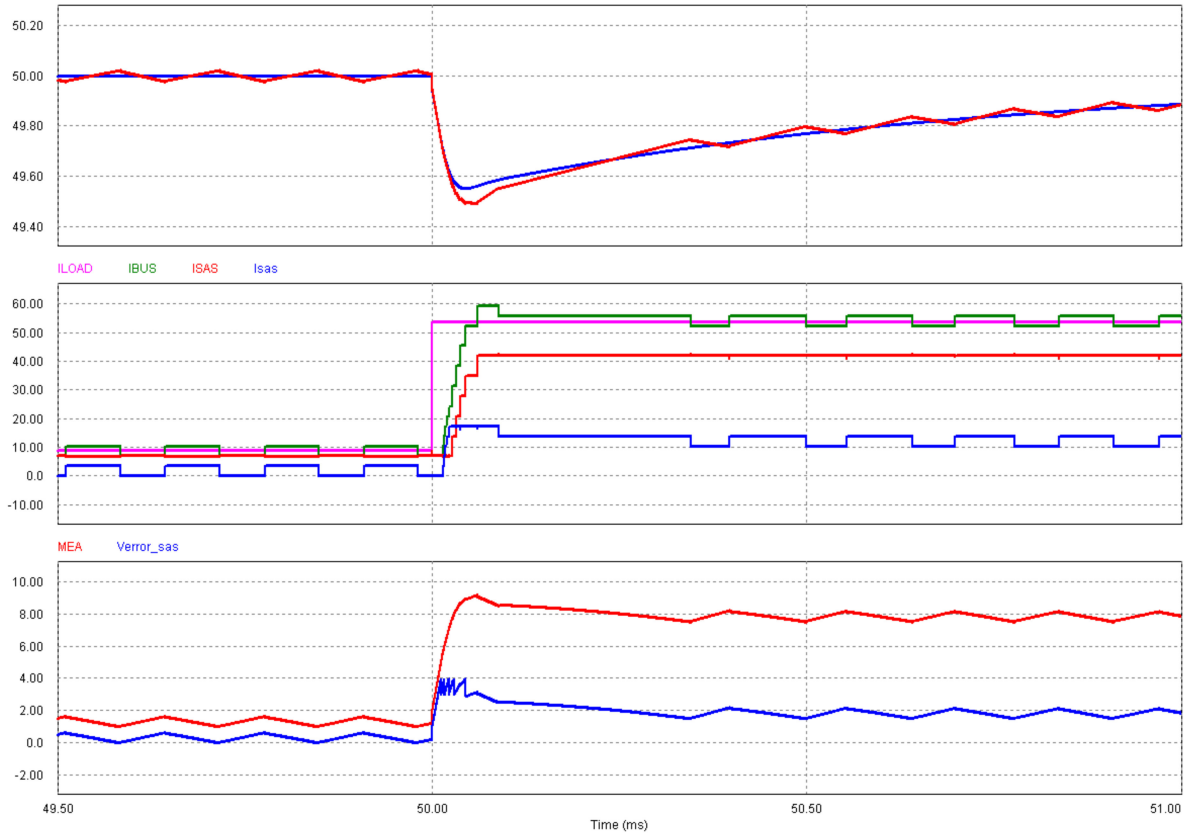

Figure 7. Simulation waveforms.

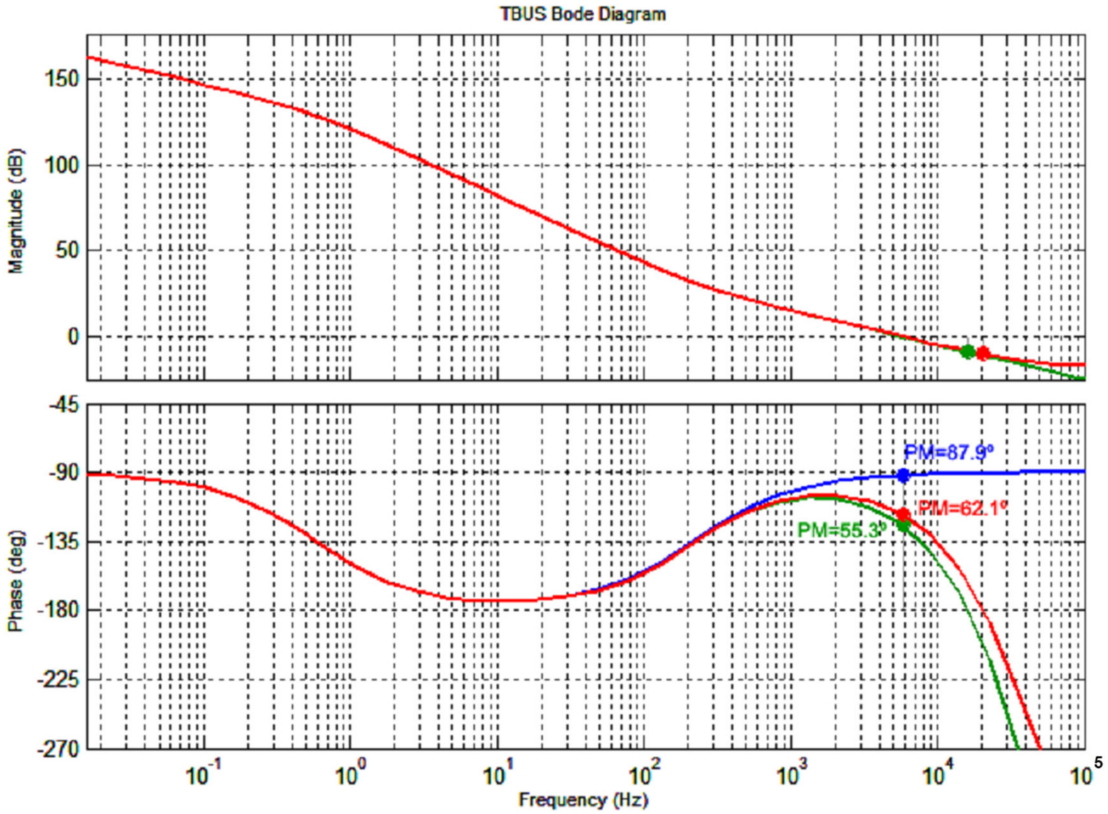

Figure 8. Simulated control loop response: blue, no delay; green, *Csa* delay; red, *Csa* delay + lead–lag network.

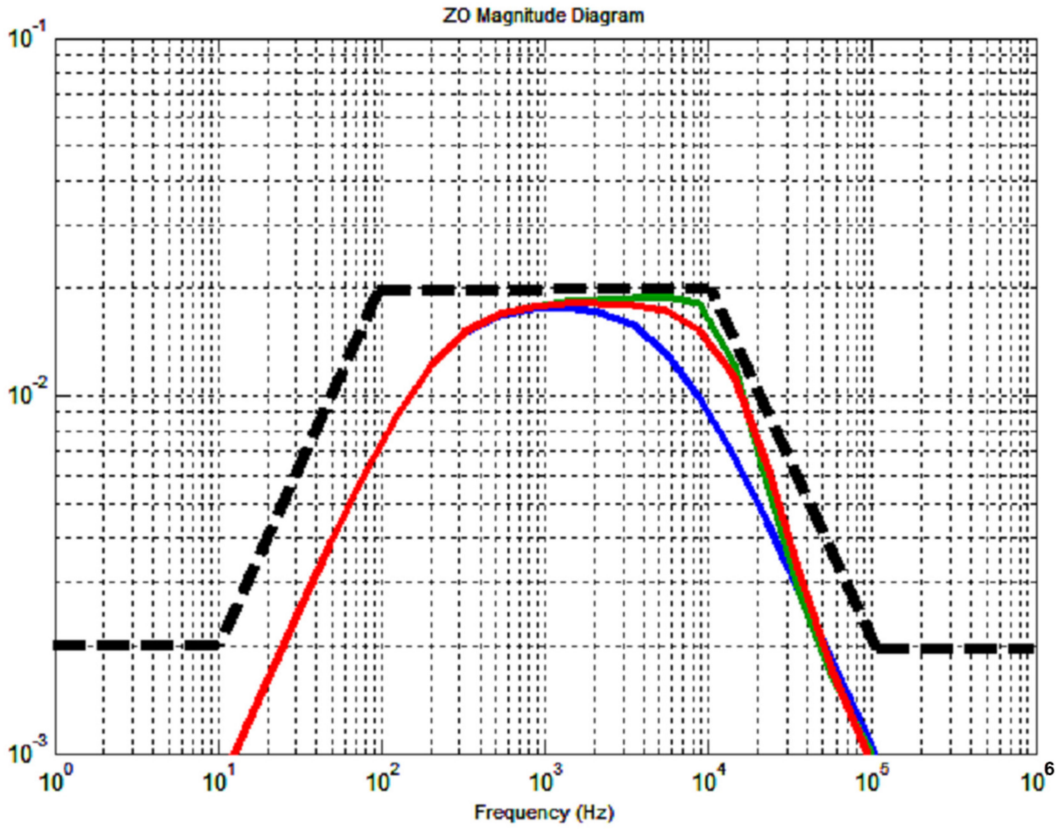

Figure 9. Output impedance simulation: blue, no delay; green, *Csa* delay; red, *Csa* delay + lead–lag network.

5. Experimental Results

Following the *ESA* standards, a low-power system was breadboarded to test the new proposed control method. The main features of the prototype are listed in Table 3.

Table 3. Breadboard system specifications.

Breadboard System Specifications	
Power	1200 W
Bus voltage (V_{BUS})	50 V
Bus voltage ripple (ΔV_{BUS})	<1% V_{BUS}
Maximum output impedance ($Z_{O\ max}$)	50 mΩ
Control loop gain margin	≥10 dB
Control loop phase margin	≥60°
High-power solar array sections	3 (4 A/section)
Low-power solar array sections	4 (1 A/Section)
Bus capacitance	480 μF

E4351B Solar Array Simulators from Keysight Technologies was used as inputs for the prototype while the load has been emulated with a DC Electronic Load N3300 from Keysight Technologies and controlled with Labview by a computer to simulate load power steps. All measurements were done with a DPO4034 four-channel oscilloscope from Tektronix.

In Figure 10, the steady-state response of the regulator is presented. In this case, the load current is set to 12.5 A, three high-power sections are fully connected to the bus and one low-power section switches to regulate the bus. The voltage spikes that can be seen in the voltage ripple are created by the switching action of the section that regulates the bus. Each time the section is shunted, the parasitic capacitance is short-circuited, and a voltage spike appears; in real systems, an active current limiter is used in each section to avoid

these voltage spikes. It is worth mentioning that the peak-to-peak voltage of these spikes was 200 mV, which is lower than the 500 mV (1% Vbus) specification.

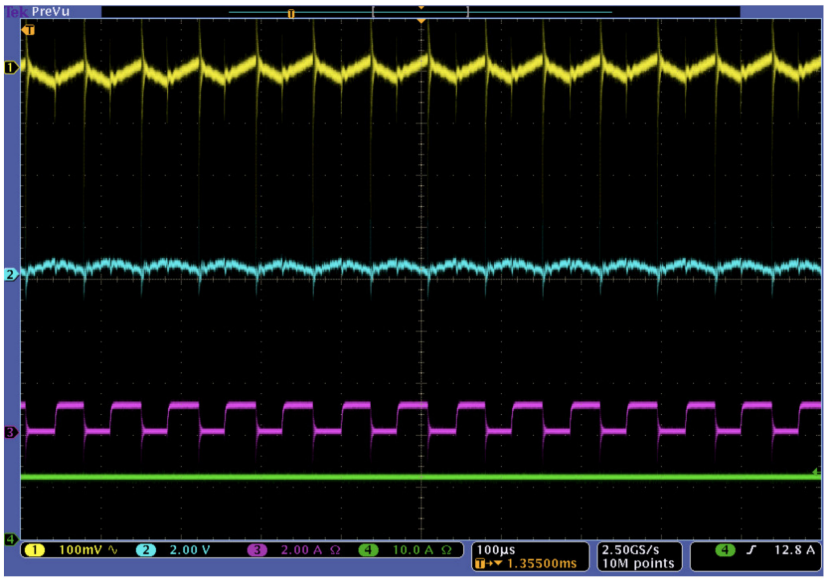

Figure 10. Experimental results (steady-state), *ILoad* = 12.5 A. Yellow, bus voltage ripple; blue, low-power sections control signal; pink, low-power sections bus current; green, high-power sections bus current.

In Figures 11 and 12, the response of the regulator to a load step of 10 A is presented. In this case, the load current changes from 2.5 to 12.5 A. When the load current is 2.5 A, two small sections are fully connected and another one switches to regulate the bus. When the load current is 12.5 A, three high-power sections are fully connected, and one low-power section switches to regulate the bus. It can be seen in the low-power section control signal how a constant voltage (2 V) is subtracted or added each time a high-power section is connected or disconnected.

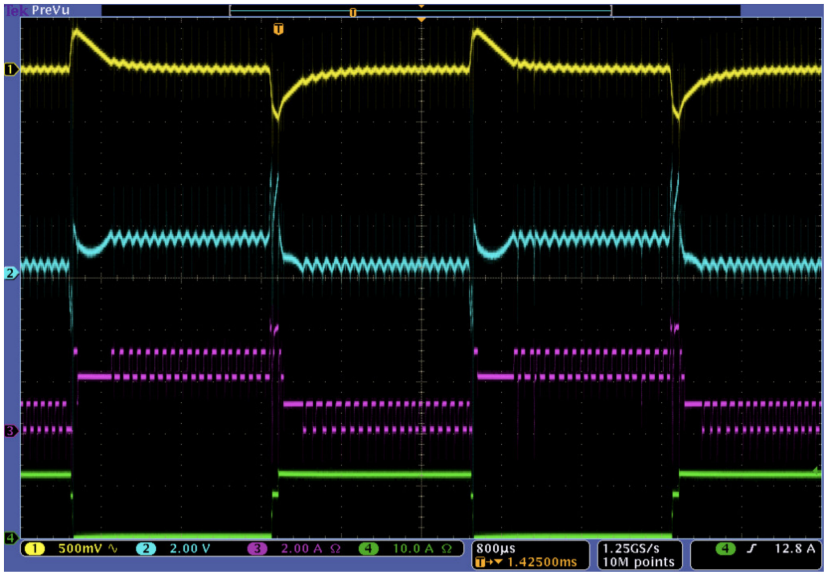

Figure 11. Experimental results (large load perturbation), *ILoad* = 2.5–12.5 A. Yellow, bus voltage ripple; blue, low-power sections control signal; pink, low-power sections bus current; green, high-power sections bus current.

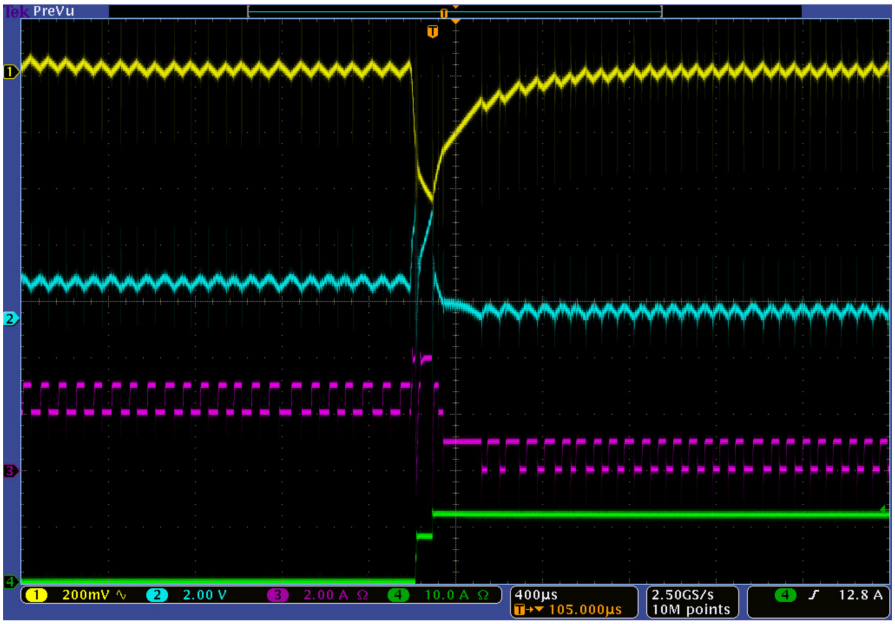

Figure 12. Experimental results (large load perturbation detail), *ILoad* = 2.5–12.5 A. Yellow, bus voltage ripple; blue, low-power sections control signal; pink, low-power sections bus current; green, high-power sections bus current.

6. Conclusions

A new S^3R control parallel power control method is presented for reducing the losses and improving the *AC* characteristics when high parasitic capacitance solar arrays are used. The proposed method was implemented in a low-power prototype and validated with different tests. This concept can also be applied to the sequential switching shunt series regulator (S^4R) [14], reducing the ripple on the battery charging current.

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