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# Interleaved, Switched Inductor and High-Gain Wide Bandgap Based Boost Converter Proposal

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**Abstract:** Many applications (electric vehicles, renewable energies, low-voltage DC grids) require simple, high-power density and low-current ripple-boost converters. Traditional step-up converters are limited when large transformation ratios are involved. In this work is proposed a step-up converter that brings together the characteristics of high gain, low ripple, and high-power density. From the converter proposal, a mathematical analysis of its operation is first performed, including its static transfer function, stress of components, and voltage and current ripples. Furthermore, it provides a design example for an application of  $V_{in} = 48$  V to  $V_o = 270$  V and 500 W. For its implementation, two different wide bandgap (WBG) semiconductor models have been used, hybrid GaN cascodes and SiC MOSFETs. Finally, the experimental results of the produced prototypes are shown, and the results are discussed.

**Keywords:** boost; switched-inductor; WBG; SiC; GaN; DC/DC; LVDC

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## 1. Introduction

In recent years, with the massive adoption of electricity as the main energy source by end users, an adaptation in voltage ratings is taking place for distribution as well as for consumption.

At the domestic and industrial level, the main promoters of change are the introduction of low-voltage direct-current (LVDC) distribution grids and the increasing use of renewable sources of energy. In this field, the proposed distribution and consumption network voltages are in the 24–380 V range [1–7]. Based on the premise that the output voltages of renewable energy sources—photovoltaic and fuel cells—are below the voltage distribution and consumption level, the use of boost converters is required [8–10].

Within the automotive sector, the latest electric vehicle configurations operate in general in the 150–450 Vdc range [11], requiring, as well, the use of step-up converters to supply voltage to the electrical engines from the batteries or to charge them [12].

The aerospace and aeronautical segments do the same. The introduction of electric propulsion systems and the transition from mechanical to electric drive systems have increased electric power consumption, thus increasing the need to use higher voltage [13–16].

In this scenario, DC–DC conversion systems play a key part, allowing the interconnection between buses and loads from energy sources.

The expected features of such converters are reliability, size, weight, and reduced current ripple. Input current ripple is particularly important in those systems where the power source is a battery or fuel cell, because of its lifetime impact [17].

To solve these requirements, different solutions can be considered taking into account the simplicity of design, implementation, and cost. In the previous mentioned applications,

non-isolated interleaved boost converters are widely used [10]. Nevertheless, there are other applications, usually related with high step-up ratios and high power, where efficiency is a major concern. Here, isolated converters are used in order to optimize efficiency and enhance the security of the system thanks to the transformer, but in counterpart volume, mass and price are increased [18,19].

A key factor in the converter selection topology is the step-up ratio. High step-up ratios using simple converters and controllers is a challenging task due to the presence of zeros in the left half-plane. This tends to unbalance the system when it operates at high duty cycles, becoming the controller more sensitive to inaccuracies and delays [20].

Although there are techniques described in the literature to minimize these effects [21,22], the use of voltage boosting techniques allows lower duty cycles, reducing the controllers complexity but at the same time increasing the number of components [23].

Low duty cycle enables simpler multidevice structures in the converters, providing several advantages: decouple the switching frequency from the inductor frequency, reduce the input current ripple, share the losses among devices and in more complex designs, enable reconfiguration techniques to improve the versatility and robustness of the converter [24].

Voltage boosting techniques can be used to reduce the duty cycle; the most popular are based on charge pumps that are well-suited for low power applications [25], the use of voltage multiplication cells that require the use of capacitors [26], and finally the use of switched inductors, based on magnetizing inductors in parallel and demagnetizing them in series [27]. In this paper, the use of switched inductors will be analyzed.

In [28] a high-gain (from 32 to 800 V), non-isolated step-up converter with interleaving is introduced. It employs voltage multiplication cells to keep a reduced duty cycle of 0.68. The converter has been evaluated in different load conditions achieving a 95% efficiency for 500 W. Another high-gain (from 20 to 260 V), non-isolated converter is presented in [29]. It uses transistor-switched inductors to achieve a reduced duty cycle of 0.75. For experimental validation, it has been evaluated at 200 W loads, achieving 94.5% efficiency.

This work proposes a high-gain interleaving boost converter scheme that uses a switched inductor for achieving high gain ratios with no need of high duty cycles. As mentioned, the switched inductor structure charges several inductors in parallel during the ON-State and discharges them in series during OFF-State.

The main strength of this proposal lies in its great versatility. A widespread structure of  $n$  interleaved phases,  $k$  phase-switched inductors and  $m$  phase-switched power transistors is developed. This allows the optimization of the inductors, the limitation of the input and output current ripple and power sharing between phases.

Considering the high step-up ratio required and with the aim of increasing power density, the prototypes have been fully developed with wide bandgap (WBG) semiconductors. The key advantages of these semiconductors—SiC and GaN—over traditional silicon devices are the Band Gap Energy, Breakdown Field, Saturation Drift Velocity and Thermal conductivity. As a result, higher voltage transistors can be produced for higher temperatures, which enables the optimization of thermal management systems—and higher frequency—which reduces the size of the passive elements [30–33].

To conclude this introduction, the paper has been structured as follows: Section 2 presents the general topology and its working concept. In Section 3, two converters are proposed, one based on SiC switches and one based on GaN switches. Section 4 presents and discusses the experimental results, and it closes with a conclusion of the work in Section 5.

## 2. Converter description and operation principle

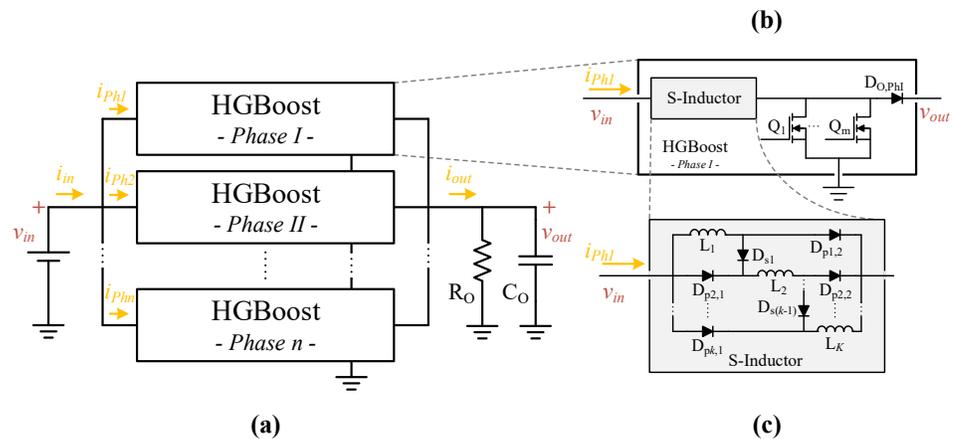
The proposed converter scheme has a multiphase high-gain boost (HGBoost) structure, as shown in Figure 1a. The benefits of this type of structure, commonly referred to as the Interleaved Boost Converter (IBC), are related to the power-sharing between phases and the reduction of the input current ripple [34,35].

According to Figure 1b, the proposal employs multiple switches per phase. The switches will turn on sequentially every  $360^\circ/m$ , where  $m$  is the number of switches per phase, sharing the power between all each period. On the other hand, there will be a phase shift of  $360^\circ/n$ , where  $n$  is the number of phases. There is an impact of this type of implementation in terms of power and current distribution between switches. The main drawback of this type of implementation is the increased complexity of the control [10].

Additionally, the proposed converter incorporates a switched inductor cell (S-Inductor) that improves the step-up voltage capability of the circuit.

A continuous current mode operation (CCM) would be considered for the HGBoost operating description [36]. Each HGBoost phase has two states, ON-State and OFF-State (Figure 2). The voltage and current waveforms in each inductor of the S-Inductor based on each of the following states is shown in Figure 3a. It is important to note that due to the interleaving, the duty cycle ( $D$ ) will be within the range  $(0, 1/m)$ , where  $m$  is the number of switches per phase.

In the ON-state, one of the transistors is turned on. Because of the S-Inductor configuration, during this interval, shown in Figure 2a, the  $k$ -inductors are connected in parallel. A small unbalance voltage appears in the inductors in parallel; the first inductor and the  $k$ -th have only one diode ( $D_F$ ) in series ( $V_F$ ) in this state, thus they have a slightly higher voltage according to the expression (1).



**Figure 1.** Simplified sketch of the proposed high-gain boost converter: (a) General diagram of the n-phase converter; (b) Single-phase scheme with  $m$  transistors; (c) Scheme of the selected switched inductor.

During the OFF-State all transistors are off and the current flows through the series diodes ( $D_s$ ), keeping them in series and supplying the load through the output diode ( $D_o$ ), according to Figure 2b. The voltage in each inductor, assuming an identical charging in ON-State of the inductors is given by (2).

$$\begin{cases} V(L)_{ON} = V_{IN} - V_F; \text{ for the first and last inductor} \\ V(L)_{ON} = V_{IN} - 2V_F; \text{ for the rest of inductors} \end{cases} \quad (1)$$

$$V(L)_{OFF} = \frac{V_{in} - V_{out}}{k} - V_F \quad (2)$$

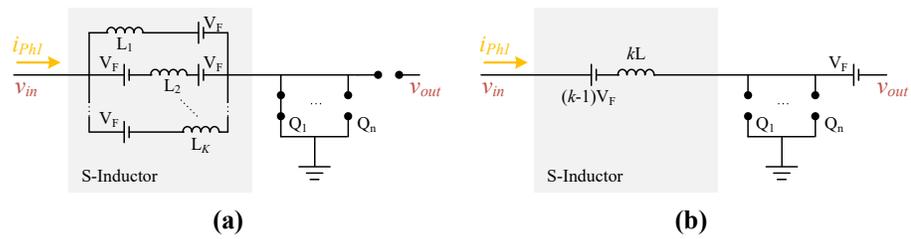


Figure 2. HGBoost equivalent states: (a) ON-State. (b) OFF-State.

Assuming identical inductances, the following DC transfer function (3) can be obtained, where  $D$  means the one-switch duty cycle,  $v_{in}$  the input voltage,  $v_{out}$  the output voltage,  $m$  the number of switches per phase and  $k$  the total number of inductors in the S-inductor. A graphic representation of the output voltage as a function of  $Dm$  for an input voltage of 48 V and different  $k$  is shown in Figure 3b.

$$V_o = V_{in} \left( \frac{1 + (k - 1)Dm}{1 - Dm} \right) - kV_F \left( \frac{1 + Dm}{1 - Dm} \right) \quad (3)$$

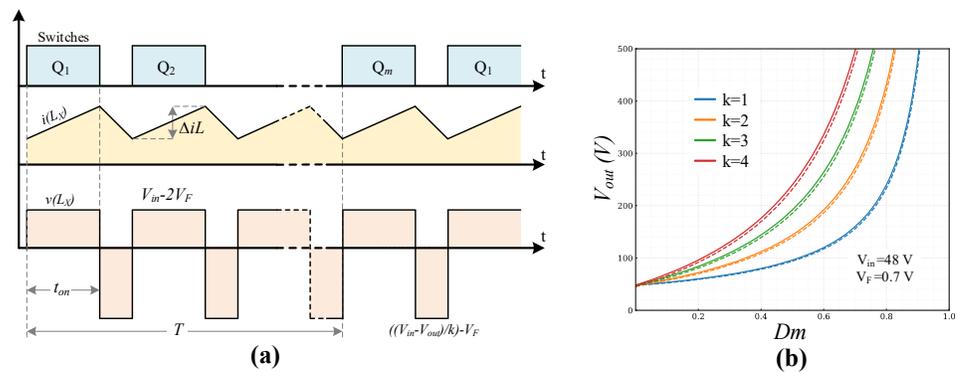


Figure 3. Waveforms and graphic transfer function: (a) Current and voltage waveforms in an inductor ( $L$ ) of one inductor from S-Inductor. (b) Graphic DC transfer function representation ( $V_o$ ) for different numbers of inductors of the S-Inductor ( $k$ ). An input voltage of 48 V and a direct diode drop ( $V_F$ ) of 0.7 V are considered. In continuous line, the drop voltage of the diodes is neglected, in dashed line, a 0.7 V voltage drop is considered.

The stress on the semiconductors will be analyzed next. The blocking voltage supported by the parallel diodes of the S-Inductor ( $D_{pi,j}$  - Figure 1c) are described in (4) and (5). It should be noted that the  $D_{pi,1}$  diode is connected to the input and the  $D_{pi,2}$  diodes are connected to the output. In all cases  $V_F$  was neglected compared to the magnitude of the input and output voltages. The maximum blocking voltage in the series diode ( $D_{si}$ ) of the S-Inductor is described by (6).

$$V(D_{Pi,1}) = \frac{i - 1}{k} (V_{OUT} - V_{IN}) \quad (4)$$

$$V(D_{Pi,2}) = \frac{k - i}{k} (V_{OUT} - V_{IN}) \quad (5)$$

$$V(D_{Si}) = V_{IN} \quad (6)$$

On the other hand, the maximum voltages supported by the switches correspond to the output voltage  $V_{DS}(Q) = V_{OUT}$ .

For the inductor current, it is possible to calculate, assuming no losses, an average current per inductor defined by (7) where  $n$  is the number of phases and  $i_o$  the output current.

$$\langle i(L) \rangle = \frac{\langle i_o \rangle}{n(1 - Dm)} \quad (7)$$

Maximum diode current corresponds with the maximum inductor current, defined according to (8). Maximum switch current is defined by (9) where  $f$  is the switching frequency.

$$I_{max}(D) = i_{max}(L) = \frac{\langle i_o \rangle}{n(1 - Dm)} + \frac{V_{in}D}{2fL} \quad (8)$$

$$I_{max}(Q) = k \left( \frac{\langle i_o \rangle}{n(1 - Dm)} + \frac{V_{in}D}{2fL} \right) \quad (9)$$

As mentioned before, an advantage of interleaving topologies is the decreasing of current ripple, (10) and (11) are the expressions for input and output current ripple are described, where

$Y = m(T - t_{on})f$  and  $X = nY$ .

$$\Delta i_{out\ RMS} = \langle i_{in} \rangle \sqrt{\frac{\left[ \left( Y - \frac{X}{n} \right) \left( \frac{X+1}{n} - Y \right) \right] + n \left[ (X+1)^2 \left( Y - \frac{X}{n} \right)^3 + X^2 \left( \frac{X+1}{n} - Y \right)^3 \right]}{12Y^2 \left( \frac{V_{in} t_{on}}{\langle i_{in} \rangle L} \right)^2}} \quad (10)$$

$$\Delta i_{in} = (k-1) \frac{\langle i_o \rangle}{n(1 - Dm)} + (k+1) \frac{V_{in}D}{2fL} \quad (11)$$

### 3. Converter Design Example:

The prototype for experimental validation is a two-phase device ( $n = 2$ ), with two switches per phase ( $m = 2$ ) and two inductors per phase ( $k = 2$ ). The voltage gain is  $V_o/V_{in} = 5.6$ , with  $V_{in} = 48$  V and  $V_{out} = 270$  V. Based on (3), this implies a switch duty cycle of 0.35. This voltage range is well-suited for a large number of applications [1,5,37–39].

Because of the high output voltage, full WBG diodes and switches have been considered. In both cases, the diodes are SiC, but SiC and GaN switches have been tested. In addition, Schottky SiC diodes minimize switching losses and make it possible to increase the switching frequency compared to silicon diodes [30].

SiC and GaN switches, due to the high voltage breaking field, can be produced using thinner wafers—compared to Si—achieving significant reductions in resistances ( $R_{on}$ ) and parasitic capacitances. In practice, this means lower switching losses [31] and also lower conduction losses, enabling the reduction of thermal management systems and increasing power density [32].

A major constraint for this use is the special driving characteristics required. On one hand, the low capacitances of the devices ( $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$ ) require layouts with minimum source inductance in order to minimize the ringing on switching [40,41]. Furthermore, and especially for GaN devices, they have a high sensitivity to gate overvoltages [40]. The latest SiC switch (MOSFET) reviews incorporate dedicated source terminals to minimize the effects of source inductance on switching [42]. Due to their gate-overvoltage sensitivity, some GaN switch manufacturers integrate transistor and controller on the same chip [43]; however, currently these devices are for 300 V and are therefore not suitable for this application.

To achieve the GaN device advantages without the driver disadvantage, hybrid devices were considered. A GaN cascode hybrid switch uses a GaN Junction Field-Effect Transistor (JFET) as the main power control device, while a conventional low-voltage Si

MOSFET is used to control it. Consequently, very balanced devices in terms of performance/drive requirements are available in the market.

The developed prototype to validate the proposal is shown in Figure 4, and the selected elements are in Table 1. To drive both transistor proposals (TP65H035WSQA and SCT3120ALHR), CREE's CPWR-AN10 driver was used. One of the advantages of this driver lies in the use of unregulated isolation sources to provide controlled ON and OFF voltages to the transistors [44] allowing the validation of both transistors without major layout changes. The manufacturers' recommended driving voltages were used [45,46]. The CPWR-AN10 includes an optoisolated inputs control, and a Zynq@-7000 Xilinx unit was used to generate the PWM control signals.

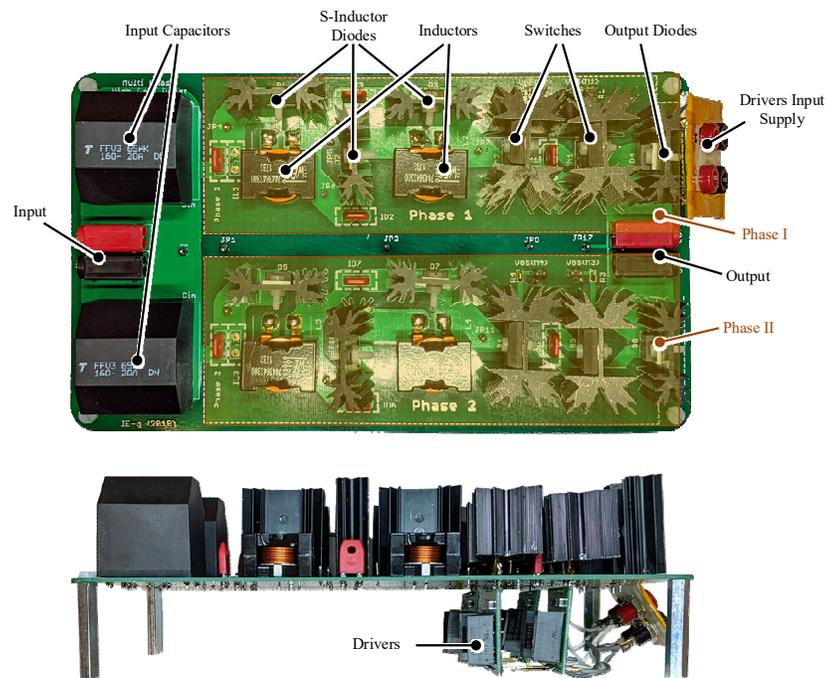


Figure 4. Top and side view of the prototype circuit.

Table 1. Parameters and elements selected in the prototypes.

Element	Value	Ref
Input Voltage – ( $V_{in}$ )	48 V	PSW 80-40.5 - GW Instek
Output Voltage – ( $V_o$ )	270 V ( $D = 0.35$ )	
Power	500 W	4x HSC200150RJ - Tyco
Inductances – (S-inductor)	33 $\mu$ H	7443643300 – WE
Diodes	SiC – 1200 V/12 A	UJ2D1210T – United SiC
Switches – ( $Q$ )	Op1: SiC – 650 V/120 m $\Omega$	SCT3120ALHR – ROHM
	Op2: GaN – 650 V/41 m $\Omega$	TP65H035WSQA – Transph.
Drivers	WBG Driver	CPWR-AN10
Input Capacitor – ( $C_{in}$ )	200 $\mu$ F	FFV34E0107K - AVX
Output Capacitor – ( $C_o$ )	590 $\mu$ F	FFVE4I0227K - AVX
Switching Frequency	100kHz	Xilinx Zynq@-7000

#### 4. Experimental Results: SiC and GaN Versions

A MDO3104 Tektronix mixed-domain oscilloscope was used as a data acquisition instrument. Tektronix TCP0030A current probes and Tektronix THDP0200 high-voltage differential probes were also used.

For its operation, the converter was controlled in open loop, through a fixed duty cycle ( $D = 0.35$ ) for a constant output voltage. The same measurements were carried out using SiC and GaN switches.

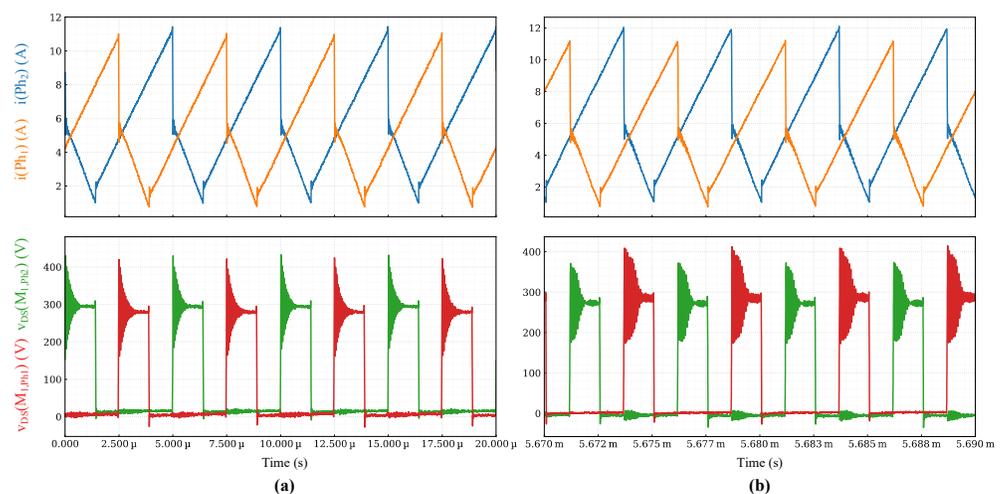
#### Phase currents and switch voltages

The phase current and the drain-source switch voltage waveforms are shown in Figure 5a for the SiC converter and Figure 5b for the GaN converter.

First, correct phase interleaving is verified. For the SiC converter, Figure 5a, a properly balanced current is verified, with a maximum current of roughly 11.3 A; this value has good correlation with (8), assuming identical inductors. In the GaN converter Figure 5b, there are 400 mA maximum current variations per phase; this may be due to the tolerance of the inductors (15%).

By means of a voltage analysis of the switches, the DC transfer function (3) is verified, as well as the output voltage, since  $V_{DS}(M_i) = V_{OUT}$ .

On the other hand, some switching ringing appears, due to resonances between the parasitic elements of the circuit [47]. However, the ringing overvoltage is within the nominal voltage of the switches (650 V) and does not represent a risk.



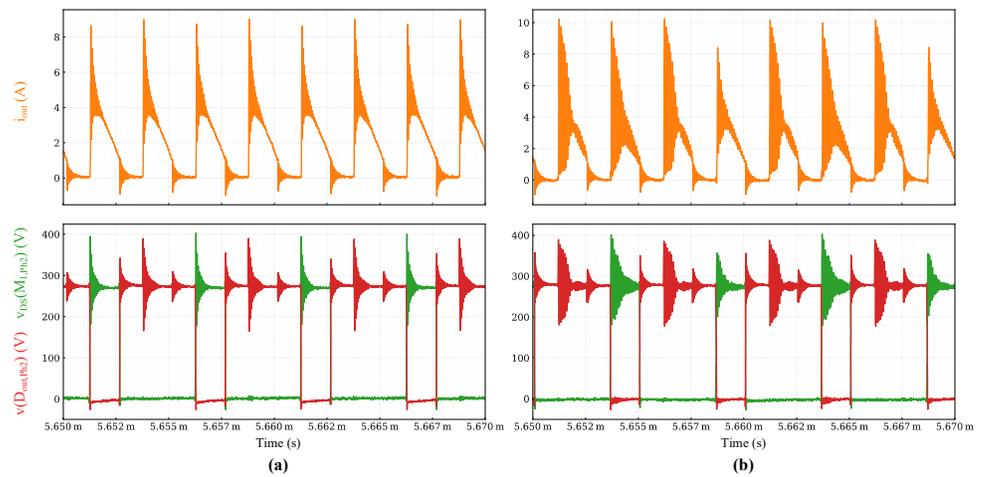
**Figure 5.** Converter waveforms: **(a)** SiC switch converter (SCT3120ALHR). Upper waveform: In orange current  $i(Ph_1)$  (2 A/div); in blue  $i(Ph_2)$  (2 A/div). Lower waveform: In green  $V_{DS}(M_{1,Ph1})$  (100 V/div); in red  $V_{DS}(M_{1,Ph2})$  (100 V/div). Time scale 2.5  $\mu$ s/div. **(b)** GaN switch converter (TP65H035WSQA). Upper waveform: In orange current  $i(Ph_1)$  (2 A/div); in blue  $i(Ph_2)$  (2 A/div). Lower waveform: In green  $V_{DS}(M_{1,Ph1})$  (100 V/div); in red  $V_{DS}(M_{1,Ph2})$  (100 V/div). Time scale 2.5  $\mu$ s/div.

#### Output currents and Output Diode Voltage

Figure 6 shows the converter output current ( $i_{out}$ ) waveform before the output capacitor ( $C_o$ ) and the single-phase output diodes voltages as well as the drain-source switch voltage for SiC Figure 5a and GaN Figure 5b prototypes.

It can be noted that the output current frequency equals twice the frequency from one switch, allowing it to reduce the voltage and current ripple.

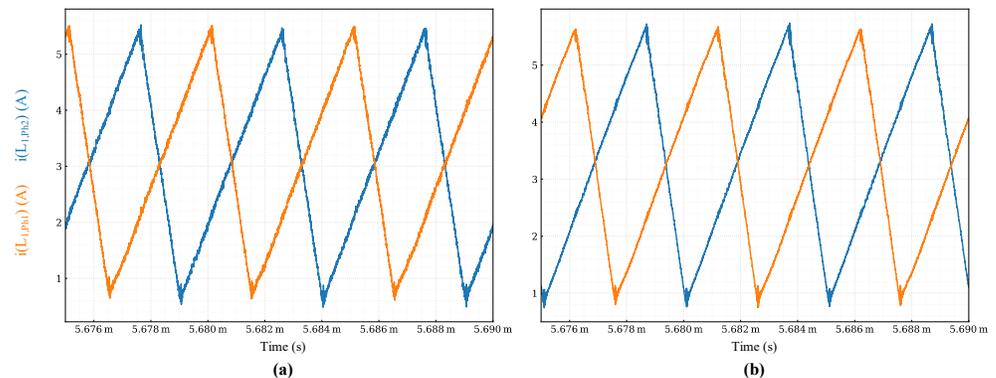
The inductor tolerance effects are shown more clearly in the GaN prototype again in Figure 6b; however, these currents are within the range of the output diodes (UJ2D1210T).



**Figure 6.** Converter waveforms: **(a)** SiC switch converter (SCT3120ALHR). Upper waveform: In orange current  $i_{out}$  (2 A/div). Lower waveform: In green  $V_{DS}(M_{1,Ph2})$  (100 V/div); in red  $V(D_{out,Ph2})$  (100 V/div). Time scale 2.5  $\mu$ s/div. **(b)** GaN switch converter (TP65H035WSQA). Upper waveform: In orange current  $i_{out}$  (2 A/div). Lower waveform: In green  $V_{DS}(M_{1,Ph2})$  (100 V/div); in red  $V(D_{out,Ph2})$  (100 V/div) Time scale 2.5  $\mu$ s/div.

### Inductor Currents

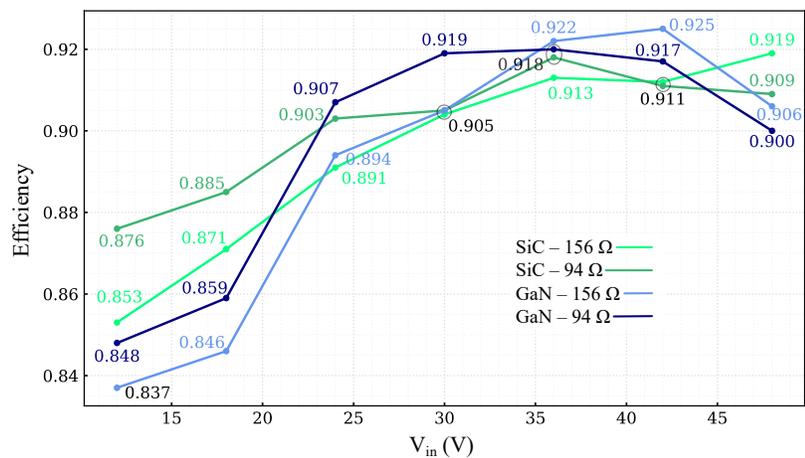
Figure 7 shows the first inductor current of each S-Inductor, Figure 7a for the SiC converter and Figure 7b for the GaN converter. It can be verified that both converters work in continuous mode with about 500 mA of margin. The maximum currents reached are in accordance with the theoretical value (8), at 5.6 A value.



**Figure 7.** Converter waveforms: **(a)** SiC switch converter (SCT3120ALHR). In orange current  $i(L_{1,Ph1})$  (2 A/div); in blue  $i(L_{1,Ph2})$  (2 A/div). Time scale 2  $\mu$ s/div. **(b)** GaN switch converter (TP65H035WSQA). In orange current  $i(L_{1,Ph1})$  (2 A/div); in blue  $i(L_{1,Ph2})$  (2 A/div). Time scale 2  $\mu$ s/div.

### Efficiency

Figure 8 shows the efficiency of the prototypes under different load conditions, 156  $\Omega$  and 94  $\Omega$ . For its operation, a fixed 0.35 duty cycle was selected and an input voltage sweep between 12 and 48 V was performed, regardless of the type of semiconductor employed (SiC & GaN).



**Figure 8.** Prototypes efficiency under different load and input voltage. In light green SiC prototype with 156  $\Omega$  load. In dark green SiC prototype with 94  $\Omega$  load. In light blue GaN prototype with 156  $\Omega$  load. In dark blue GaN prototype with 94  $\Omega$  load.

## 5. Conclusions

An interleaved high-gain boost converter based on a switched inductor able to provide high-gain ratio for operation in low-voltage DC networks and automotive power systems has been presented and validated in this paper. The main advantage of the proposal is its high versatility, allowing power sharing between phases and switches, and reducing the current ripple.

The equations provide three adjusting parameters,  $m$  (number of switches per phase),  $k$  (number of switched inductors per phase), and  $n$  (number of phases). Thanks to its high level of configurability, the proposal's design can cover a wide range of step-up voltages and power ratings.

For its validation, two 500 W converters with  $48V_{in}$  and  $270V_o$  were designed; a two-phase device ( $n = 2$ ), with two switches per phase ( $m = 2$ ) and two inductors per phase ( $k = 2$ ) were selected.

The experimental results based on the use of SiC and GaN switches show very uniform results from the point of view of switching response as well as efficiency. Since the evaluated WBG devices have different driving voltages, the use of an adjustable voltage driver (CPWR-AN10) was possible to validate the design with both switches without driver changes.

For future works, it would be interesting to evaluate the operation using soft switching techniques to increase efficiency and to suggest synchronous rectification techniques to minimize the impact of the diodes.

**Author Contributions:** D.M., A.G. and J.M.B. conceived the idea, designed the experiment, guided the experiment, and wrote the manuscript; R.G., C.T. and C.O. conducted most of the validation test. All authors have read and agreed to the published version of the manuscript.

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