Self-Powered 380 V DC SiC Solid-State Circuit Breaker and Fault Current Limiter

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***Abstract*—This paper presents a new ultrafast dc solid-state circuit breaker (SSCB) that uses a silicon carbide cascode as the main switching and limiting semiconductor and an isolated photovoltaic driver to control it. The proposed topology is self-powered and fully implemented with discrete parts. The SSCB's cascode can work in three different states—fully ON during nominal operation, linear mode for current limitation, and fully OFF to disconnect the load. The time the SSCB operates in linear mode and the maximum current limit is easily set by discrete components. Control inputs have also been included to reset the SSCB after a fault has been removed or to remotely switch it ON or OFF. This device can be used in dc distribution avoiding deterioration due to the problems associated with electric arcs and mechanical aging of moving parts, limiting inrush currents and also minimizing conduction losses respect other kind of circuit breakers. Functional, thermal, and efficiency tests have been carried out with three different 380 V prototypes. Experimental results show the excellent behavior of the SSCB, it is able to block a 380 V short circuit failure in 570 ns; the authors have not found any faster results in the literature.**

***Index Terms*—DC power distribution, fault current limiter, silicon carbide (SiC) cascode, solid-state circuit breaker (SSCB), wide-bandgap semiconductors (WBG) semiconductors.**

I. Introduction

ALTHOUGH ac is the dominant form of electric power distribution, dc distribution systems are becoming more and more popular [1], [2]. The main reason is the progressive change of the type of loads connected to the main grid. Currently, dc loads, such as LED lights, computers, communications, and battery chargers, need an ac/dc converter as a first stage to be connected to the ac grid, increasing power losses and costs [3]. Therefore, direct dc power distribution is an interesting option for systems with large amount of dc electronics loads and, in recent years, it has been successfully applied in shipboards, airplanes, telecommunication systems, buildings, electric vehicle charge stations, and data centers [1]–[7].

Focusing on data centers, the increase in cloud computing and Internet services has driven an exponential increase of their electric consumption. Nowadays, data centers consume about 3% of the world's electricity production and it is estimated that it will double every five years [8]. Most of the data center loads are computers, servers, routers, switches, and storage devices, which are dc loads. Besides, the uninterruptible power supply, required for critical situations, is based on batteries. In many papers, dc distribution has been proposed for this application [8]–[11], reducing the conversion steps and total losses, resulting in more efficient, reliable, and economic data centers. Among all the proposals, 48 and 380 V dc distributions have been the two most promising alternatives to the conventional ac distribution. Between these two alternatives, previous studies show that the 380 V dc option is better than 48 V as it has higher efficiency and lower costs [10].

As in ac systems, protection devices are also needed in 380 V dc distribution systems in order to provide protection against overloads and faults. In [11], a three-level protection hierarchy architecture for 380 V dc data centers is proposed where the lower level is the individual protection with a circuit breaker (CB) of each 2 U (380 V-2.5 A) or 4 U (380 V-3.5 A) server. However, the lack of cost-effective dc protection solutions remains a major barrier, hindering the transition to efficient 380 V dc power distribution [12].

There are some important issues in dc system protection that must be considered when designing these protection devices [13]–[15].

1) Arcing at the moment of disconnection: This issue is not important in ac systems because of the naturally zero crossing of the ac current, but in dc systems it is very important to have a method that assures that the load current is zero before the physical disconnection of the load from the grid.
2) DC loads usually have a high input capacitance to filter high-frequency harmonics caused by switching dc–dc converters. The inrush current associated with this capacitance may cause unexpected CB trips when the load is first connected to the dc distribution system. On the other hand, it is important to limit this inrush current because it can cause voltage sags affecting other loads.
3) The high distributed capacitance in the dc bus deals in very fast and high discharge currents in case of low impedance load or short-circuit. This issue will affect other loads if the fault is not isolated very fast.

In the market, it can be found that traditional mechanical dc circuit breakers with different current ratings. However, these breakers cannot deal with the issues previously listed because

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of their slow response time, low lifetime due to the arcing, and their lack of current limiting capability [2], [16]. In the literature, some dc solid state circuit breakers (SSCB) based on power semiconductors have been also proposed [14]–[18]. They are very attractive due to their ultrafast current interruption, arcless interruption, and current limiting capability. However, their main drawback is the conduction losses due to the semiconductor on resistance during nominal operation. As an alternative, hybrid solutions have also been proposed [19]–[22], using a mechanical switch in parallel with a semiconductor device allows low power losses, arcless interruption, current limiting, and reasonable interruption speeds, but they are more complex and expensive.

The advent of new silicon carbide (SiC) semiconductors has reactivated the option of using SSCBs [23]–[31]. The main reason is that SiC devices have lower conduction resistance than their silicon counterparts, besides their thermal impedance is better, and also they can work at higher junction temperatures, reducing the risk of failure due to high junction temperature. Performance evaluation of multiple Si and SiC devices for circuit breakers in 380 V dc systems have been reported in [24] and [25], concluding that 1200 V SiC devices are the best option for this application, and presenting a 5 A/380 V design based on a normally ON SiC junction field-effect transistor (JFET). The main drawback of using a normally ON device is that the driver has to be carefully designed to assure that the breaker trips off in a fault condition. The proposed solution is quite complex and it needs a high ratio buck dc–dc converter to power the driver and a digital signal processor to control the circuit. In [30], a 12.5 A/400 V SiC-based circuit breaker is presented; its novelty is based on a control method of the gate voltage to reduce the overvoltage across the semiconductor during the interruption process. The gate signal is generated by a digital signal controller and a high-speed D–A converter with its ancillary power supply is also needed to sense the current.

In this paper, a simple ultrafast self-powered SSCB and fault current limiter based on a SiC JFET cascode for 380 V dc distribution systems are presented.

The rest of the paper is organized as follows. Section II introduces the proposed circuit and its principle of operation. Section III describes the experimental prototype and the most relevant results obtained. The paper concludes with Section IV.

II. Proposed SSCB

The proposed SSCB is based on a SiC cascode and an isolated photovoltaic driver to generate the floating gate-source voltage needed to control it. The cascode works fully ON during nominal operation, in linear mode for current limitation and fully OFF to disconnect the load. The proposed circuit is shown in Fig. 1, it is self-powered and has been fully devised with discrete parts.

The SSCB is divided into the following functional blocks.

A. Main Semiconductor

As commented earlier, the circuit is based on a SiC cascode (M_1) controlled by an isolated photovoltaic driver (PV_1).

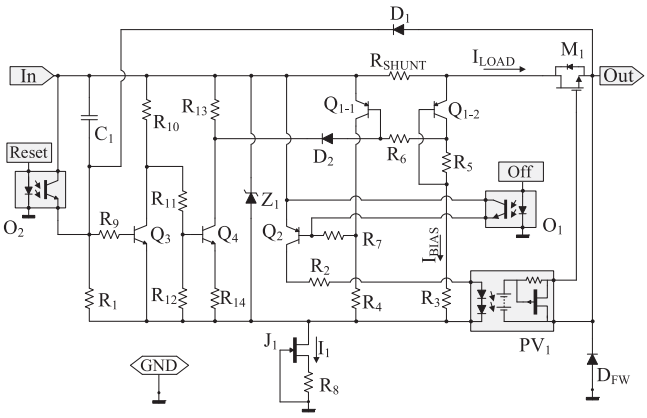

Fig 1. Electrical schematic of the proposed SSCB.

B. Current Sensor

It is made up by the current measuring resistor R_{SHUNT}, the two matched transistors Q_{1-1}, and Q_{1-2}, the biasing resistors R_3 and R_4, and the gain resistor R_5.

C. Timer and Latching Circuit

The time constant given by the R_1–C_1 network sets the time in which the SSCB operates in linear mode (latching time), limiting the current to a preconfigured maximum value after a failure is detected and before the load is fully disconnected. If the fault extinguishes before the latching time, the circuit returns to its nominal operation. The latching circuit R_9, R_{10}, R_{11}, R_{12}, R_{13}, R_{14}, Q_3, Q_4, and D_2 provides a precise transition from the current limiting mode to OFF mode (open circuit).

D. Biasing Zener and Current Source

The protection is self-powered, it is supplied directly from its input, the 380-V bus, without needing auxiliary sources. Z_1 acts as an internal power supply and sets the proper voltage for the current sensor, timer, and latching circuit. Thus, these circuits are also referred to as Zener voltage, minimizing power losses and voltage stress. A current source, J_1 and R_8, is used for Z_1 biasing. To minimize the J_1 thermal stress, the current flowing through it must be minimized. The losses of the current source are given by

$$W_{J_1} = V_{J_1} \cdot I_{J_1} \approx (V_{\mathrm{In}} - V_{Z_1}) \cdot I_{J1}. \tag{1}$$

E. Driver

An isolated photovoltaic driver (PV_1) is used to control the SiC cascode, M_1. This solution offers the following advantages over other isolated driver circuits: high electrical isolation capability, do not require external power supply, it provides direct analog voltage to operate the main cascode in linear mode, simple fast turn-OFF circuits could be used (often integrated in the driver), and finally, low photo-cell current enables naturally slow turn-ON (especially attractive for inrush current control).

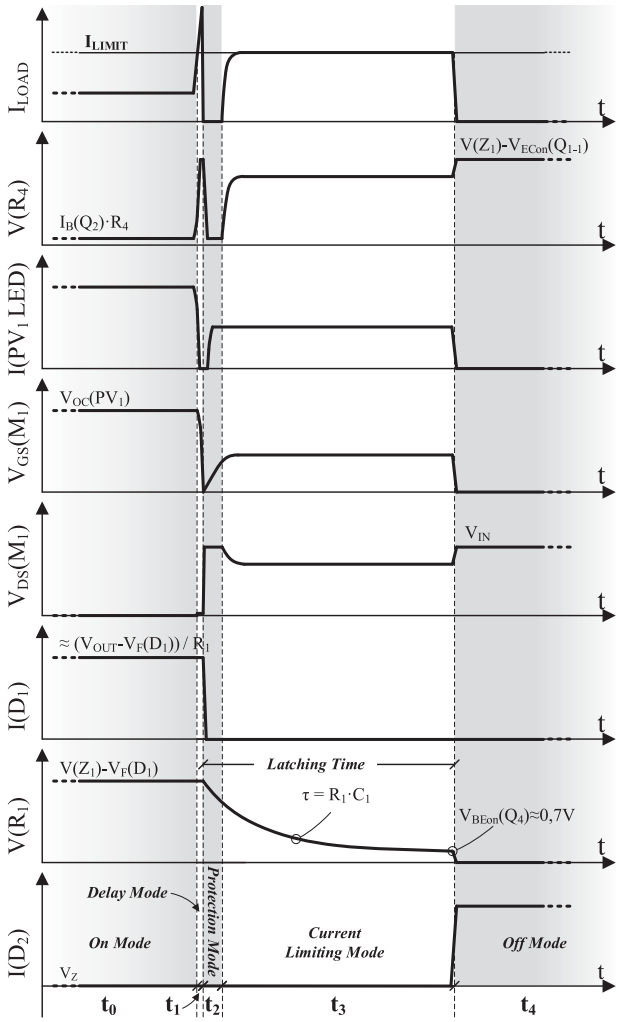

Fig 2. Most important voltage and current waveforms during overload. From top to bottom: load current, $V(R_4)$, PV_1 LED current, $V_{GS}(M_1)$, $V_{DS}(M_1)$, $I(D_1)$, $V(R_1)$, and $I(D_2)$.

PV_1 primary LED current is controlled by Q_2 transistor and it will be drained through J_1, so the current through J_1 is $I_{J1} \approx I_{Z1} + I_{PV1}$.

F. Remote Reset and Turn Off

Two optoisolated inputs (reset and OFF) have been included to control the SSCB. The reset input is used to reconnect the SSCB from the OFF mode. It is performed discharging C_1 (latching circuit). Besides, the OFF control input forces the SSCB to disconnect the load, opening Q_2 and disconnecting the power supply to PV_1.

G. Freewheeling Diode

Finally, the SSCB includes a freewheeling diode (D_{FW}) to handle inductive loads and prevent overvoltage in M_1.

The SSCB operation is explained below with the help of Fig. 2. Five different operation modes are identified: ON mode, delay mode, protection mode, current limiting mode, and OFF mode.

- *t_0—On Mode*

In this mode, the cascode, M_1, is fully ON, supplying the required current to the load, I_{LOAD}. The equivalent circuit in this state is shown in Fig. 3(a). The voltage drop on R_{SHUNT} is not enough to activate Q_{1-1}, so Q_2 remains saturated, allowing a current flow through the primary LED of the photovoltaic driver (PV_1) and therefore providing at the driver output the open circuit voltage [Voc (PV_1)] to M_1 gate-source voltage. D_1 is also in ON-state, keeping Q_3 switched ON and the timer capacitor, C_1, discharged. The Q_{1-2} current, named I_{BIAS}, is defined by

$$I_{BIAS} = \frac{V(Z_1) - I_{LOAD} \cdot R_{SHUNT} - V_{EB}(Q_{1-2})}{R_3}. \quad (2)$$

The circuit will stay in this state until I_{LOAD} reaches the necessary current level to activate Q_{1-1}. In this case, naming I_{LIMIT} the maximum I_{LOAD} current. This current limit I_{LIMIT} is given by the following equation:

$$I_{LIMIT} = \frac{I_{BIAS} \cdot R_5}{R_{SHUNT}} = \frac{(V(Z_1) - I_{LIMIT} \cdot R_{SHUNT} - V_{EB}(Q_{1-2})) \cdot R_5}{R_3 \cdot R_{SHUNT}}. \quad (3)$$

where $I_B(Q_{1-1})$ and $I_{B(Q_1-2)}$ have been neglected and it is assumed $V_{EB}(Q_{1-1}) = V_{EB}(Q_{1-2})$.

Assuming $V(Z_1) >> (I_{LIMIT} \cdot R_{SHUNT} + V_{EB}(Q_{1-2}))$, the current limit threshold is finally approximated by

$$I_{LIMIT} \approx \frac{V(Z_1) \cdot R_5}{R_3 \cdot R_{SHUNT}}. \quad (4)$$

- *t_1—Delay Mode*

Just after the load current exceeds the current limit, the SSCB starts a very short delay interval in which it does not limit current. As it can be observed in Fig. 2, as soon as Q_{1-1} is activated, Q_2 is turned OFF and the PV_1 LED current is removed fast; however, M_1 capacitances must be discharged before the SSCB is able to limit the current. The equivalent circuit is shown in Fig. 3(b). This delay time depends on the driver turn-OFF circuit and the M_1 characteristics.

- *t_2—Protection Mode*

Once M_1 capacitances are discharged, it is turned OFF, protecting the main dc bus and isolating the faulty load as fast as possible. Besides, Q_{1-1} is turned OFF and Q_2 saturates, allowing again a current flow through the primary LED of PV_1. Nevertheless, the cascode continues OFF until the driver output voltage exceeds the threshold voltage, at this moment the SSCB will enter in current limiting mode. The increase of $V_{DS}(M_1)$ forces D_1 to turn OFF and the timer circuit starts charging C_1. The protection mode time depends on the driver turn-ON circuit and the M_1 characteristics. The equivalent SSCB is shown in Fig. 3(c).

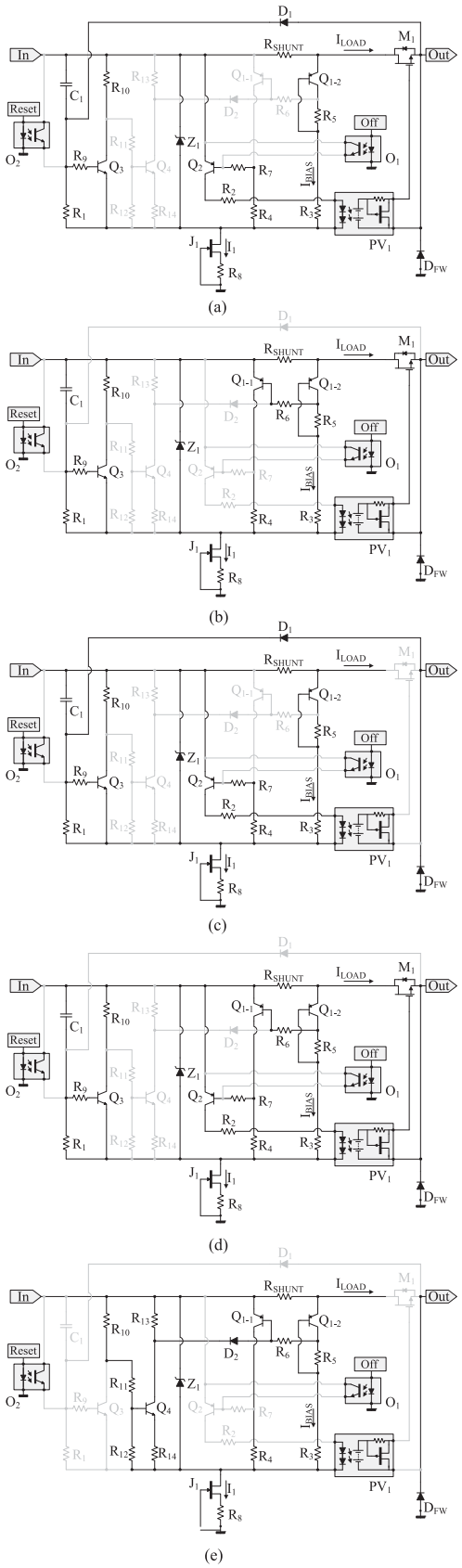

Fig 3. SSCB equivalent state circuits. (a) Equivalent circuit during ON mode operation. (b) Equivalent circuit during delay mode. (c) Equivalent circuit during protection mode. (d) Equivalent circuit during current limiting mode. (e) Equivalent circuit during OFF mode.

- t_3—*Current Limiting Mode*

Current limiting mode refers to that mode of operation in which the circuit maintains a constant current at a predefined value (I_{LIMIT}). After the fault has been isolated, the current feedback loop performed by R_{shunt}, Q_{1-1}, Q_{1-2}, and Q_2 increments $V_{\mathrm{GS}}(M_1)$ dealing in a linear operation of the main cascode limiting the load current to the current limit threshold (I_{LIMIT}). The voltage balance given by (3) forces Q_2 to regulate the PV_1 LED current, which generates the proper gate-source voltage from the driver photocells. The low short-circuit current of the driver ensures a very slow M1 switch-ON dynamic, thus preventing oscillations and instabilities in the SSCB. The equivalent circuit of the SSCB during this time interval is shown in Fig. 3(d).

The SSCB remains in current limiting mode until Q_3 turns OFF and Q_4 turns ON. This time (t_{latching}) is adjusted by the timer circuit, R_1–C_1. Latching time is finally given by

$$t_{\mathrm{latching}} = R_1 \cdot C_1 \cdot \ln \frac{V(Z_1) - V_F(D_1)}{V_{EB}(Q_3)} \tag{5}$$

where it is assumed $R_9 >> R_1$. This mode can also be used to limit the inrush current associated with the load input capacitance. Therefore, the latching time must be carefully designed depending on the type of loads.

If the fault (or an inrush current) extinguishes before the latching time, Q_2 will be turned ON again, supplying PV_1 and thereby turning ON M_1. This returns the SSCB to the previous state (ON mode), otherwise the circuit will enter in OFF mode.

- t_4—*Off Mode*

If the fault remains active, after the predefined latching time, Q_3 turns OFF and Q_4 turns ON. As soon as Q_4 turns ON, D_2 also switches ON and forces Q_{1-1} to saturation. During this time, R_6 limits $I_C(Q_{1-2})$, avoiding variations in the I_{LIMIT} value. Then, Q_2 turns OFF, removing completely the PV_1 LED current. The SSCB remains latched through Q_{1-1}, D_2, and Q_4, needing an external input signal (reset) to be restarted. In this state, the corresponding circuitry is as shown in Fig. 3(e).

III. Experimental Results

To verify the theoretical developments, three different SSCBs have been designed and implemented. The SSCBs have been designed for a 380 V dc distribution system with different maximum load current limits (1.5, 2.7, and 4.4 A), assuming a 50-μF maximum load input capacitance and adjusting the latching time so they can deal with the inrush current needed to charge this capacitance. The main characteristic of the three designed SSCBs is shown in Table I.

USCi's UJC1206K cascode has been selected as the main power semiconductor controlled by the photovoltaic driver Vishay's VOM1271. A SiC JFET cascode has been selected instead of a SiC MOSFET because the ON resistance is lower in devices with similar current and voltage ratings. The UJC1206K (60 mΩ) versus C2M0080120D (80 mΩ) are representative devices, the use of the cascode represents an improvement of 25%

TABLE I
DESIGNED SSCB BASICS CHARACTERISTICS

SSCB	Theoretical Parameters
Solid State Circuit Breaker 1 (*SSCB 1*)	**I_{Limit} = 1.5A** R_2=10kΩ ; R_3=51kΩ ; R_4=51kΩ R_5=86Ω ; R_7=50kΩ ; $V(Z_1)$=10V R_{SHUNT}=0.01Ω ; $V_{EB}(Q_{1\text{-}2})$=0.7V **Latching Time = 22ms** R_1=180kΩ ; C_1=47nF ; $V(Z_1)$=10V $V_F(D_1)$=0.7V ; $V_{BE}(Q_4)$=0.7V
Solid State Circuit Breaker 2 (*SSCB 2*)	**I_{Limit} = 2.7A** R_2=10kΩ ; R_3=51kΩ ; R_4=51kΩ R_5=147Ω ; R_7=50kΩ ; $V(Z_1)$=10V R_{SHUNT}=0.01Ω ; $V_{EB}(Q_{1\text{-}2})$=0.7V **Latching Time = 15ms** R_1=180kΩ ; C_1=33nF ; V(Z_1)=10V $V_F(D_1)$=0.7V ; $V_{BE}(Q_4)$=0.7V
Solid State Circuit Breaker 3 (*SSCB 3*)	**I_{Limit} = 4.4A** R_2=10kΩ ; R_3=51kΩ ; R_4=51kΩ R_5=240Ω ; R_7=50kΩ ; $V(Z_1)$=10V R_{SHUNT}=0.01Ω ; $V_{EB}(Q_{1\text{-}2})$=0.7V **Latching Time = 10ms** R_1=180kΩ ; C_1=22Ω ; $V(Z_1)$=10V $V_F(D_1)$=0.7V ; $V_{BE}(Q_4)$=0.7V

Bold entities are the starting point for the rest of calculations presented in Table I.

TABLE II
UJC1206K AND VOM1271 MAIN ELECTRICAL CHARACTERISTICS (DATASHEET)

UJC1206K		**VOM1271**	
Parameter	Value	Parameter	Value
V_{DS} max	1200V	Typ. Input Current	10mA
I_D max	38A @25ºC 24A @100ºC	Photo-Cell OC Voltage	8.4V @10mA
$R_{DSon\ (max)}$	60mΩ	Photo-Cell SC Current	15µA @10mA
V_{GSth}	4.9V	Isolation Voltage	4500V
Ciss	2214pF		

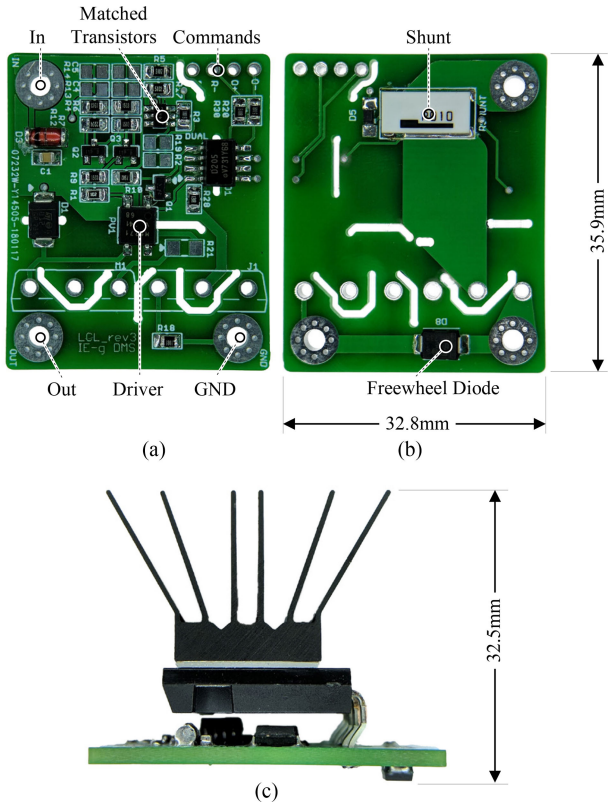

Fig 4. SSCB prototype. (a) Top view without cascode and JFET. (b) Bottom view without cascode and JFET. (c) Lateral view.

in conduction losses. Furthermore, SiC cascode behavior under short circuit condition is better than SiC MOSFET [32].

It is worth noting that in case of short circuit failure the cascode selected will operate out of the Safe Operation Area defined in the datasheet, but the aim of this paper is limited to demonstrate the correct behavior of the proposed topology. Other component should be chosen or the latching time/limit current should be reduced for long-term reliability.

Refer to Table II for the most relevant electrical characteristics of the power cascode and the photovoltaic driver. The voltage reference is obtained from a 10 V Zener diode (Z_1). The biasing source J_1-R_8 uses an USCi's UJN1205K JFET and has been adjusted to 10 mA in order to minimize power losses (estimated losses around 3.7 W). R_3 has been set to 51 kΩ, obtaining $I_{\rm BIAS}$ = 180 μA and $R_{\rm SHUNT}$ is 10 mΩ. A DMMT5401 dual matched p-n-p transistor has been selected for Q_{1-1} and Q_{1-2}. The other relevant parts have been varied depending on each particular test (see Table I).

The electronic main board of the implemented SSCBs and the final prototype is shown in Fig. 4. A black anodized heatsink is used to reduce the cascode and JFET working temperature.

Regarding the experimental setup, a Keysight N8937A high-voltage, high-power supply units have been used (1500 V; 10 A). The electrical load consists of a power bank of ten resistors (Multicomp, MC14683, 100 Ω, 225 W, and wire-wound). It has 1 kW nominal power capability at 1 kV with 1.95 mH parasitic series inductance (measured). Resistor shunting is possible using MOSFETs and a digital controller to produce step load variations.

A. Test I: Switch on Limiting Inrush Current

In this test, all SSCBs are switched ON in real working conditions. The supply voltage is 380 V, and a 400-Ω load is connected at the output in parallel with a 50 μF capacitor. The SSCB is initially in OFF mode, in t = 0 s, the SSCB is changed to ON mode using the reset remote control. After reset, as the load capacity is discharged, the SSCBs run under a short-circuit condition. As shown in Fig. 5, due to the slow dynamics of the M_1 gate charging process, no overshooting of the current is produced. The SSCB reaches its maximum current while charging the load input capacitor. For the conditions analyzed, the necessary time for charging the input capacitor is shorter than $t_{\rm latching}$ (5). Therefore, the SSCB does not change from current limiting mode to OFF mode, remaining in ON mode supplying the load.

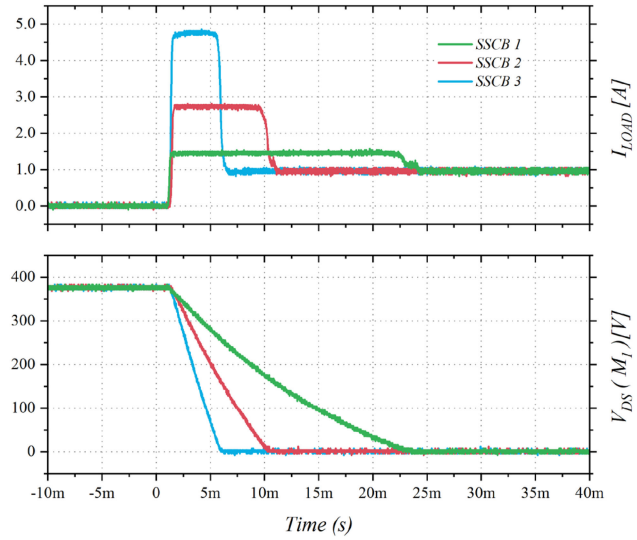

Fig 5. SSCB start limiting inrush current. Start with *R–C* load (400 Ω—50 μF) at 380 V. Upper figure: Load current (I_{LOAD}) (1 A/division). Lower figure: Main cascode drain–source voltage [$V_{\mathrm{DS}}(M_1)$] (100 V/division). Time scale: 5 ms/division.

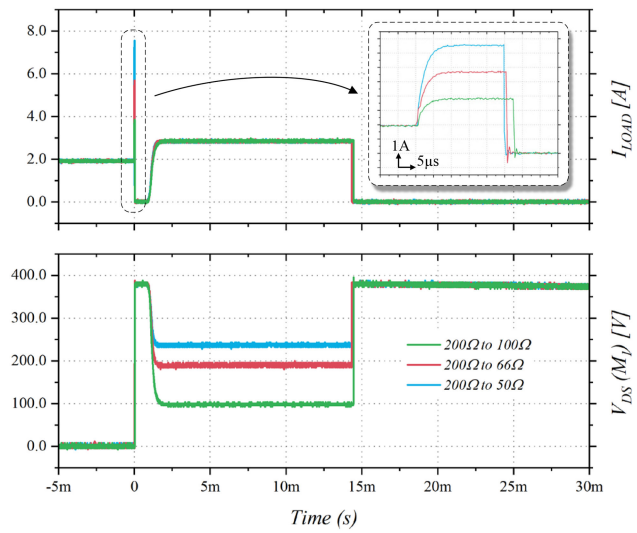

Fig 6. SSCB 2 overload sweep waveforms from 200 Ω to [100, 66, 50] Ω at 380 V. Upper figure: Load current (I_{LOAD}) (2 A/division). Lower figure: Main cascode drain-source voltage [$V_{\mathrm{DS}}(M_1)$] (100 V/division). Time scale: 5 ms/division.

B. Test II: SSCB 2 Overload Sweep

In this test, the SSCB 2 as a representative sample, has been used. Different overload levels have been carried out with a 380 V input voltage. A pure resistive load of 200 Ω is initially available, and three different step loads (100, 66, and 50 Ω) are performed in order to exceed the maximum current thresholds.

For the conditions analyzed, the necessary time for charging the input capacitor is shorter than t_{latching} (5). Therefore, the SSCB does not change from current limiting mode to OFF mode, remaining in ON mode supplying the load. After that, the SSCB initiates a controlled start-up up to the $\mathrm{I_{LIMIT}}$ current (2.75 A). Finally, after the latching time, the SSCB disconnects the load from the source.

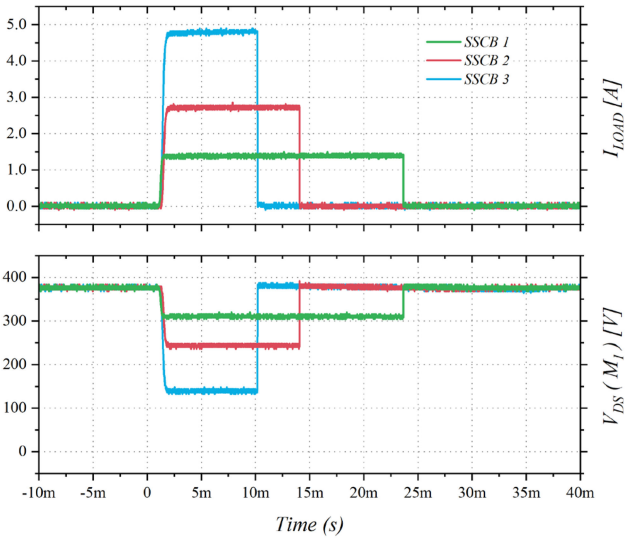

Fig 7. SSCB overload start waveforms. Start with pure resistive load (50 Ω) at 380 V. Upper figure: Load current (I_{LOAD}) (1 A/division). Lower figure: Main cascode drain–source voltage [$V_{\mathrm{DS}}(M_1)$] (100 V/division). Time scale: 5 ms/division.

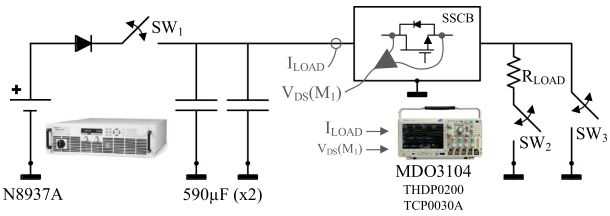

Fig 8. Short circuit test setup.

C. Test III: Overload Start

In this test, the three SSCBs are started under constant overload conditions. The input voltage is 380 V and a pure resistive load of 50 Ω is available, resulting in a 7.6-A current demand, higher than I_{LIMIT} of each SSCB. As in Test I, the SSCBs are in OFF mode state and are started with the reset command in $t = 0$ s. The results of the tests are shown in Fig. 7. The SSCBs start and immediately operate in current limiting mode providing the maximum current to the load. Finally, the load is disconnected after the latching time.

D. Test IV: Short Circuit Protection

This test validates the SSCB behavior in the worst-case scenario, a short circuit failure. SSCB 2 has been selected as the representative sample for this purpose. A dedicated setup has been designed for this test (see Fig. 8). In order to test the short circuit failure, the sequence is as follows: First of all, two 590 μF capacitors (947D591K132DJRSN—Cornell Dubilier) are charged at 380 V via $\mathrm{SW_1}$. When the capacitors are charged, $\mathrm{SW_1}$ is switched OFF and the capacitors are connected to the load (300 Ω/1.3 A) through $\mathrm{SW_2}$. The short circuit is carried out by switching ON $\mathrm{SW_3}$ 6 ms later.

Fig. 9 shows the results obtained from nominal operation to the end of the test. The SSCB is able to block the short circuit in 570 ns. In this time, a peak current value of 35 A is reached,

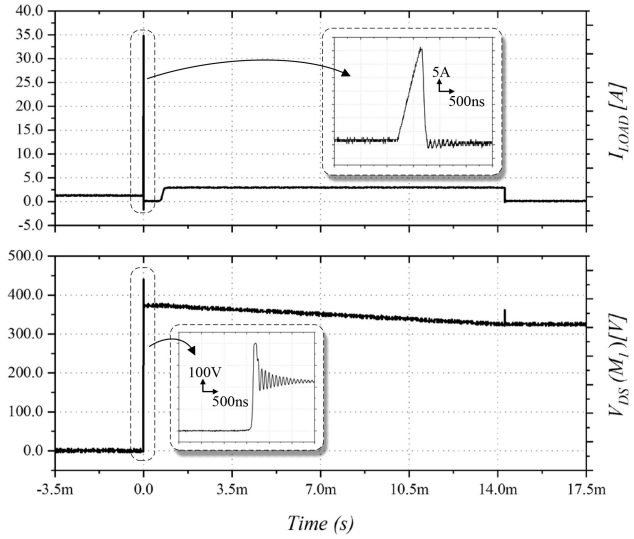

Fig 9. SSCB short circuit test waveforms. 300 Ω to short circuit. Upper figure: Load current (I_{LOAD}) (5 A/division). Lower figure: Main cascode drain-source voltage [$V_{\mathrm{DS}}(M_1)$] (100 V/division). Time scale: 3.5 ms/division.

this value is limited by the set-up parasitic inductance (approximately 5 μH). The overvoltage generated in the drain-source voltage of the cascode due to its parasitic source inductance can also be observed. After the current is removed, the SSCB starts in current limiting mode and remains until the latching time ends and the load is fully disconnected, isolating the failure from the main dc bus.

In this test, the cascode turn-OFF time is faster than VOM1271 datasheet specification. In authors' opinion, this is due to the effect of the voltage across the cascode source parasitic inductance on the fast turn-OFF circuit included in the driver.

E. Test V: Remote Reset-Off Control signals

Remote controls have been evaluated using SSCB 2 as the representative sample. Fig. 10 shows the results. The input voltage is 380 V and 200-Ω load is initially available, the load presents an input capacitance of 50 μF.

At $t = 0$ s, a step load to 50 Ω occurs, so the load current exceeds the threshold (2.7 A). After the latching time, the SSCB 2 disconnects the load from the source. At $t = 75$ ms, the overload is removed, but the SSCB remains in OFF mode. At $t =$ 100 ms the remote reset control is used and the SSCB is reset to its initial operating condition, carrying out a controlled start-up. At $t = 300$ ms, the remote OFF control is used, then the SSCB immediately blocks the current and remains in OFF mode until the input supply is removed or reset command used.

In addition to all the experimental tests shown, SPICE simulations were also performed. The simulation results exhibit good agreement with experimental measurements. Table III summarizes theoretical, simulation, and measurements results of the latching time and I_{LIMIT}.

F. Test VI: Efficiency and Thermal Analysis

In this test, the SSCB is evaluated from the efficiency and thermal management perspective. SSCB 3 has been chosen as a representative sample due to its higher power range. The tests have been carried out under nominal operating conditions, the input voltage is 380 V for all cases. The theoretical efficiency expression of the SSCB is determined as follows:

$$\eta \approx 1 - \frac{\mathrm{W_{J_1}} + (\mathrm{I_{LOAD}})^2 \cdot \mathrm{R_{DSon}}}{P_{\mathrm{IN}}}. \tag{6}$$

The efficiency of the SSCB as a function of the output power is shown in Fig. 11. For this purpose, with 380 V constant input voltage, a discrete load sweep has been carried out, the efficiency has been measured with a Yokogawa WT1800 precision power analyzer.

The thermal images shown in Fig. 12 are taken with a Fluke Industrial Thermal Imager TI450. The results are from SSCB 3

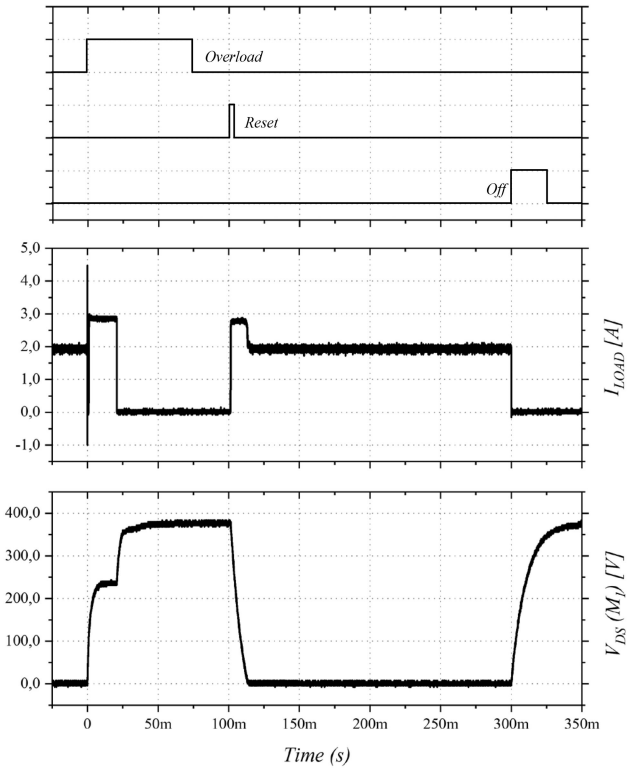

Fig 10. Remote reset-OFF control signals. Upper figure: Control signals. Center figure: Load current (I_{LOAD}) (1 A/division). Lower figure: Cascode drain–source voltage [$V_{\mathrm{DS}}(M_1)$] (100 V/division) Time scale: 50 ms/division.

TABLE III
SUMMARIZED THEORETICAL, SIMULATION, AND MEASUREMENT RESULTS

SSCB		I_{Limit}	$t_{latching}$
SSCB 1	Theoretic	1.5A	22ms
	Simulation	1.52A	21.8ms
	Measured	1.45A	22.5ms
SSCB 2	Theoretic	2.7A	15ms
	Simulation	2.64A	14.9 ms
	Measured	2.75A	12.5ms
SSCB 3	Theoretic	4.4A	10ms
	Simulation	4.34A	9.9 ms
	Measured	4.75A	8.75ms

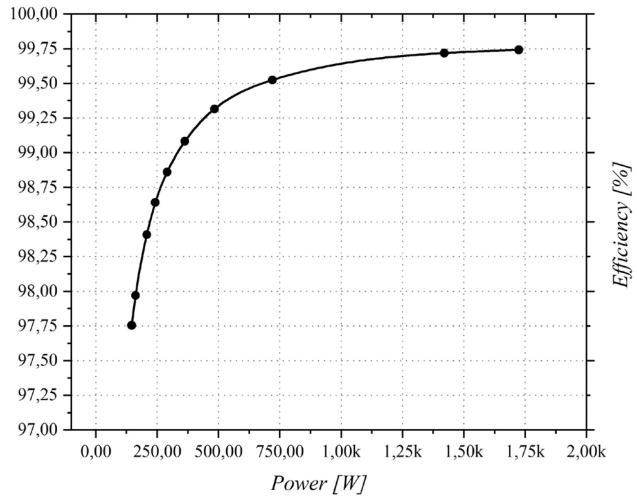

Fig 11. Efficiency versus power in SSCB 3 with 380 V input supply.

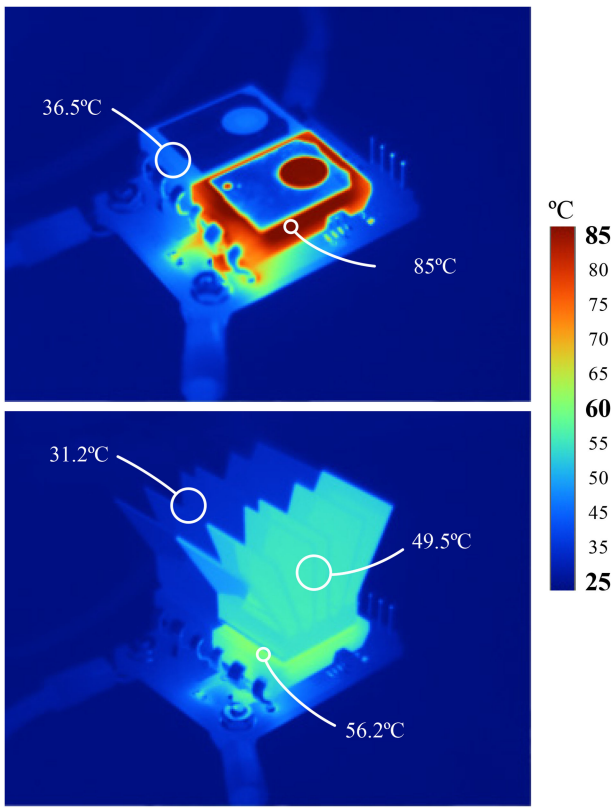

Fig 12. Real thermal performance in temperature and humidity-controlled conditions (25 °C and 15%). Upper figure: SSCB 3 at 380 V – 100 Ω without heatsink. Lower figure: SSCB 3 at 380 V – 100 Ω with heatsink.

with a 100-Ω load and 380-V supply. The upper image (without heatsink) was carried out after only one minute of operation and the J_1 temperature was still raising. The lower image (with heatsink) was carried out once J_1 was thermally stable. The environmental conditions were controlled in a thermal stabilized chamber at 25 °C and 45% relative humidity.

IV. Conclusion

In this paper, a new topology for SSCBs is presented. The proposed SSCB is able to limit inrush currents, disconnect faulty loads and also allows remote control to reset the SSCB after a fault has been removed or to switch it ON or OFF for safely connection and disconnection of the loads. The SSCB is self-powered and fully implemented with discrete parts. A SiC JFET cascode has been selected instead of a MOSFET because the ON resistance is lower in devices with similar current and voltage ratings.

Three prototypes for 380 V dc data center applications have been tested, demonstrating the good behavior of the proposed SSCB. The presented design can be extrapolated to other voltage/current levels for other applications.

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