Towards higher current and voltage LCLs

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***Abstract*— LCLs are widely used devices for power control and distribution in satellites. Traditionally, P-type MOSFETs have been used due to their simplicity from the control perspective. Actual ESA standard defines LCLs up to class 10 (10A) and 50V. However, 100V bus voltage is common in high power platforms and the current trend is to increase even more this value, around 300V. In this new scenario, the classic concept of LCL design needs to be revised, and this work proposes a simple alternative for P-type MOSFETs that operates at high voltage and can be easily scaled up in current.**

Keywords—LCL, PDU, cascode, 300V, SiC, JFET, WBG.

I. INTRODUCTION

In European satellites, Latching Current Limiters (LCLs) are the most commonly used devices for power distribution [1], see Fig.1. Typically, LCLs have been implemented using P-type MOSFETs (pMOS) as the primary power disruption device, mainly due to the simplicity of pMOS driving. However, this type of power semiconductor does not easily allow the implementation of high-voltage and high-power LCLs. A hypothetical class 2-100V LCL, considering the current criteria [2], would require four paralleled best-in-class available space-grade pMOS [3] to maintain an acceptable voltage drop in conduction mode.

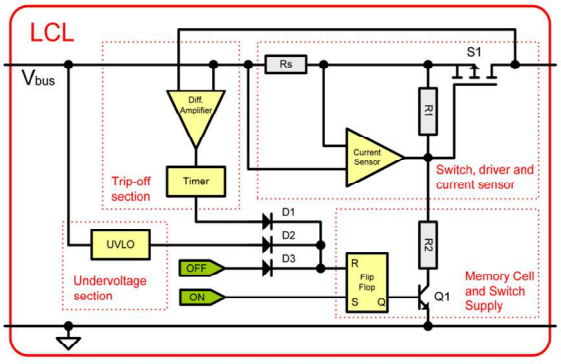

Fig. 1. LCL generic block diagram. Reproduced from [1].

The use of N-type MOSFETs (nMOS) reduces conduction losses and enables higher voltage operation. However, such implementations have the drawback of being more complex systems [4], [5].

Present Wide Band Gap (WBG) semiconductor technologies, in particular SiC, offer high performance in terms of voltage blocking capability, low turn-on loss (R_{DSon}) and high temperature operation [6]–[8].

Although few SiC diodes have already been qualified for space applications [9], there are no qualified SiC-nMOS mainly due to their lower radiation tolerance which limits their use to maximum voltages of 150V [10].

In addition, some studies suggest that the reliability of normally-on SiC JFETs in the presence of heavy ions is comparable to SiC diodes. Furthermore, other studies indicate that normally-on JFETs are, of all SiC power devices, the most stable to gamma radiation and heavy ions [10]. However, the main drawback from the designer's point of view is its normally-on nature. The way to have normally-off devices using SiC JFETs is to combine them with a Si nMOS in a cascode configuration, but the high-side driving issues still remain. To combine the advantages of pMOS driving and the high-voltage and robustness of SiC JFET, the authors have proposed a Si pMOS / SiC JFET cascode arrangement for LCL applications, and have validated for class 2-100 V devices, [12].

The aim of this paper is to continue with this development and increase in terms of current (class 6-100V) and voltage (class 3-300V), as well as start High Temperature Life Test (HTOL) campaign. Table I shows a comparison of the static characteristics of the best-in-class high voltage P-type MOSFET, a first generation SiC JFET, and a common pMOS. These values reveal that with the pMOS-SiC JFET arrangement a x2 improvement in R_{DSon} and x6 in V_{DSmax} is achieved.

TABLE I: ELECTRICAL CHARACTERISTICS
HV P- MOSFETS VS SIC JFET + LV P-MOSFET

Parameter	IRHNA597260 [HV p-MOSFET]	UJN1205K [SiC JFET]	SI4459ADY [LV p-MOSFET]
R_{DSon}	0.102 Ω	0.045 Ω	0.0039 Ω
		0.049 Ω	
$\|V_{DSmax}\|$	200 V	1200 V	30 V

II. THE P-TYPE SIC JFET CASCODE LCL

The proposed LCL circuit is shown in Fig.3, J_1 is the SiC JFET and M_1 the low-voltage pMOS. Z_2 and D_2 limit J_1 source-gate voltage, $V_{SG\text{-}J1(max)}$, and, M_1 source-drain voltage, $V_{SD\text{-}M1(max)}$.

Z_1 provides the voltage reference to the circuit, and C_1 allows smooth start-up and stabilise the reference voltage. Z_1 is biased by a current source consisting of Q_1, Q_2, Q_3, R_2, R_3 and R_4. Q_2 commands the on and off. Z_1 bias current must be kept as small as possible to minimise power losses in the current source (this is particularly important in 300V devices). Typical values are less than 1mA.

R_{shunt} together with Q_8, Q_9, R_9 and R_{10}, is the classical current limitation circuit found in many designs [1]. The limitation current (I_{lim}) is defined by (1) where the sensing bias current is given by (2).

$$I_{lim} = \frac{I_{R_{10}} \cdot R_9}{R_{Shunt}} \quad (1)$$

$$I_{R_{10}} \approx \frac{V_{Z_1} - 2V_{BE}}{R_{10}} \quad (2)$$

Trip-off time (t_{limit}) changes depending on the load fault severity. During current limitation, $V_{DS\text{-}J1}$ is monitored by the current mirror Q_{7a}, Q_{7b} and R_7, and this current is copied in a Widlar current source formed by Q_{6a}, Q_{6b} and R_5. As Q_5 conducts during current limitation, I_{R5} becomes the timer current that charges the timer capacitor (C_2) and determines t_{limit} (3).

$$t_{limit} \approx \frac{3V_F(D_1) \cdot C_2}{I_{R_5}} \quad (3)$$

R_6 sets the maximum limitation time in case of light overloads. R_8 and C_3 improves stability and avoids start-up issues. D_{FW} is a freewheeling diode for inductive loads. An sketch of the main LCL waveforms is shown in Fig.2.

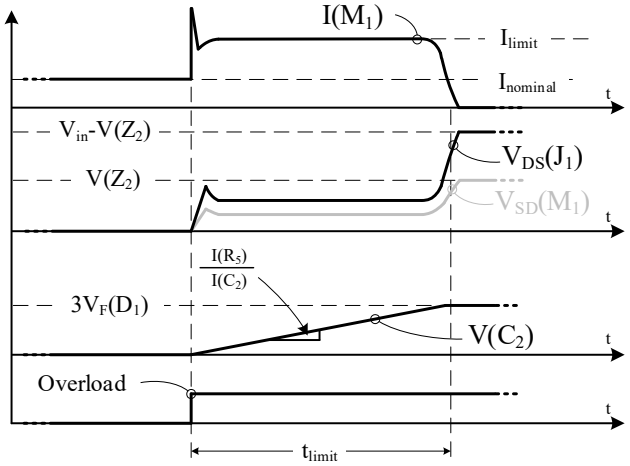

Fig 2. Sketch of the main LCL waveforms. Top: LCL current. Middle up: JFET and pMOS voltage. Middle bottom: Timer circuit voltage. Bottom: overload indicator.

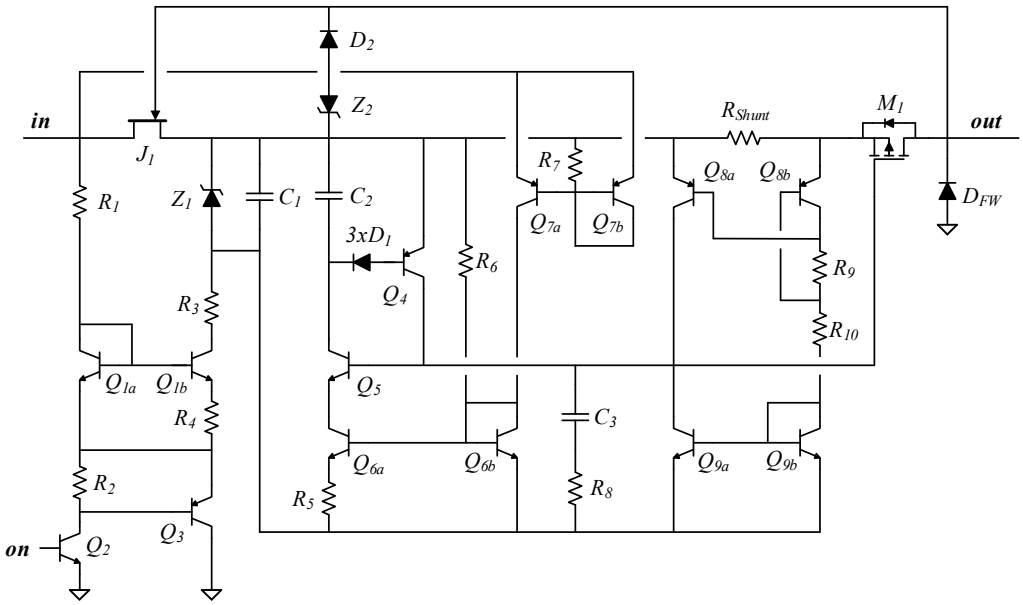

Fig 3. P-type cascode LCL implemented schematic.

III. CLASS 6 @ 100V

Table I shows that low-voltage pMOS exhibits a R_{DSon} one order of magnitude less than SiC JFET. This fact suggests the parallelization of SiC JFETs but keeping a single control pMOS to increase the class of the LCLs, as represented in Fig.4(a).

To validate the parallelisation concept for high current LCLs, a class-6 100V prototype has been implemented, please refer to Fig.4. Detailed part list is shown in Table II.

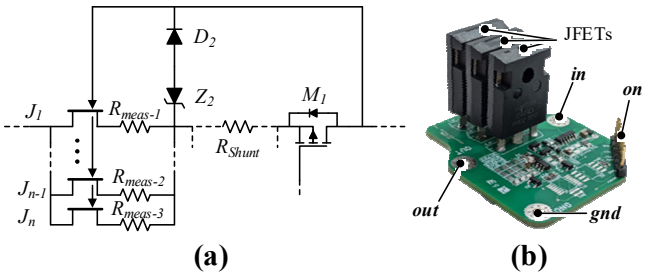

Fig 4. **(a)** Applied concept to increase LCL class while maintaining one low-voltage pMOS as control device. **(b)** Class 6 LCL prototype implemented for concept validation.

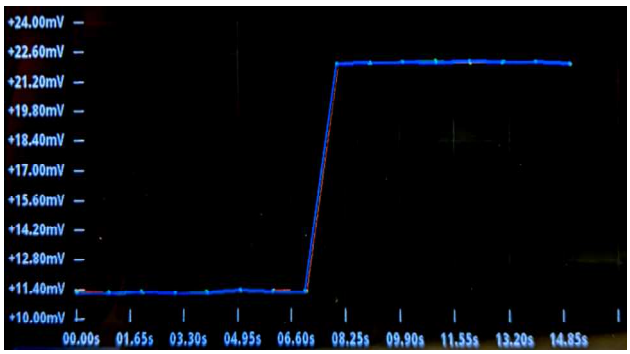

Fig 5. JFET current sharing for 3.3 A and 6.6 A load current (traces are overlapped). R_{meas} current measuring.

TABLE II:
LCL CLASS 6 @100V - PART LIST

Part	Ref	Part	Ref
J1, J2, J3	UJN1205K	**Q8**	MMDT5401
Z1	9.1 V	**Q9**	MMDT5401
D1	BAS521Q	**R1**	60 kΩ
D2	BAS521Q	**R2**	11 kΩ
Rshunt	10 mR	**R3**	11 kΩ
M1	SI4459ADY	**R4**	10 Ω
DFW	512-ES2D	**R5**	0 Ω
Z1	10 V	**R6**	100 kΩ
Q1	MMDT5551	**R7**	510 kΩ
Q2	BC817	**R8**	470 kΩ
Q3	BC807	**R9**	300 - 330 Ω
Q4	BC807	**R10**	30 kΩ
Q5	BC817	**C1**	1 uF
Q6	MMDT5551	**C2**	1 uF
Q7	unmounted	**C3**	4.7 nF

Preliminary current sharing tests in nominal operation have been performed. For the experimental validation, a 10 mΩ current sense resistor has been included in series with each JFET, R_{meas} in Fig. 4(a). As it can be observed in Fig 5, the three JFETs share properly the LCL current (traces overlapped) for 3.3 A and 6.6 A load current.

For the first overload test, the following configuration has been considered, I_{lim} = 7A and t_{limit}=15ms (Q_{7a} and Q_{7b} have been removed to set the maximum t_{limit}). It is worth to note that t_{limit} is almost x4 times the maximum value indicated in [1].

Fig. 6. shows oscilloscope screenshots under different fault load current, 8 A, 9 A and 10 A. It is clearly observed that the LCL works as expected.

To test the most severe configuration of a class-6 LCL, I_{lim} has been increased to 8 A and 8.3 A. Fig. 7. shows the oscilloscope screenshots with these two configurations under 10A overload. Reaction time is slightly affected but not the rest of results.

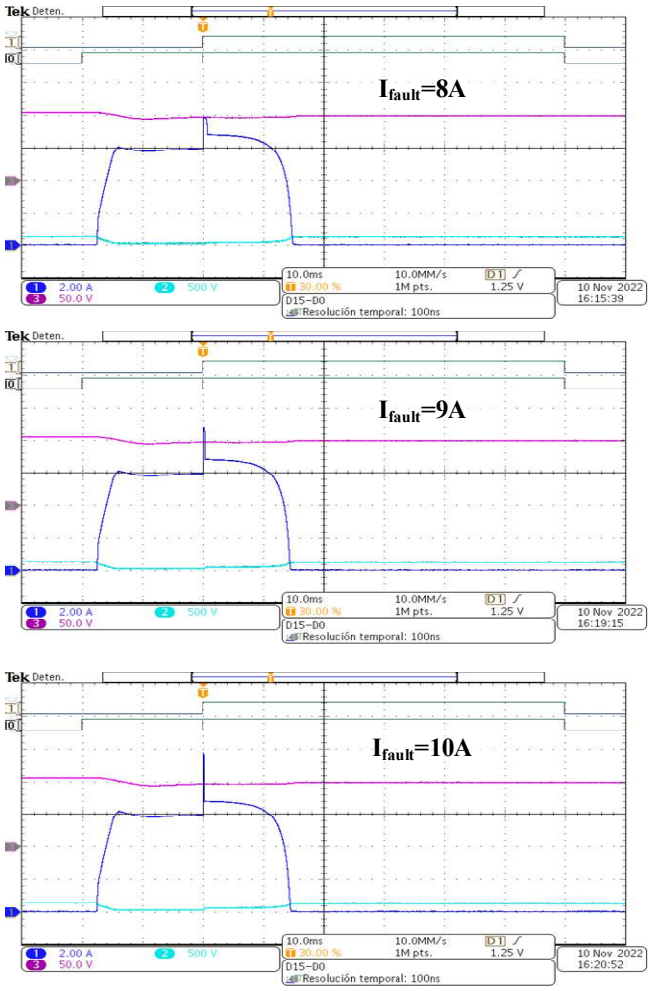

Fig 6. Operation of the class 6 LCL under an overload of 8 A, 9 A and 10 A. In dark blue LCL current (M_1), in light blue JFET V_{DS} JFETs, in magenta bus voltage.

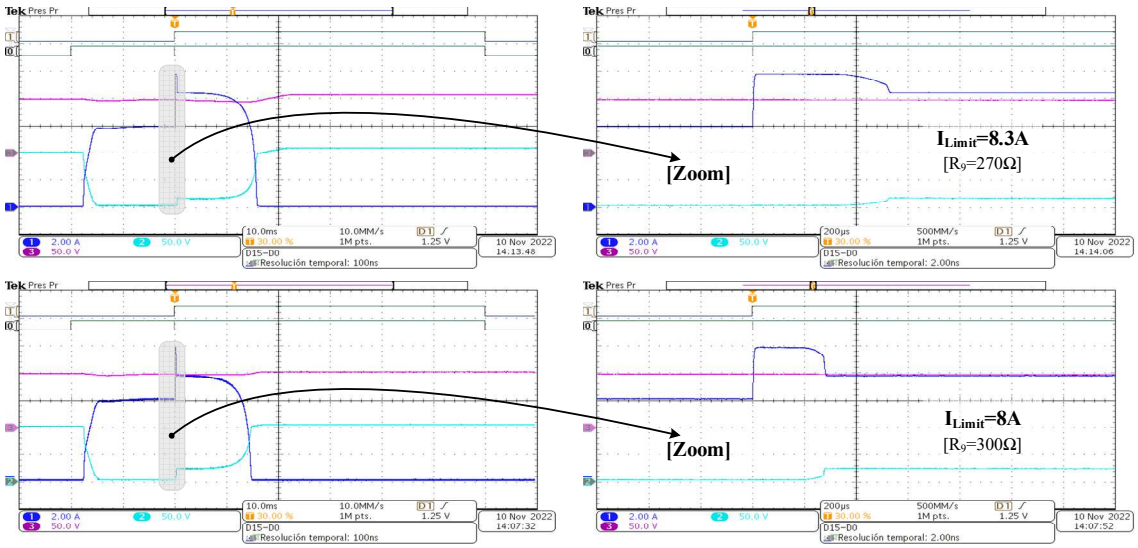

Fig 7. Operation of the class 6 LCL under an overload of 10 A and I_{lim} 8 and 8.3 A. In dark blue LCL current (M_1), in light blue JFET V_{DS}, in magenta bus voltage. Zoom views are shown in the right pictures.

IV. Class 3 @ 300V

One of the biggest challenges for high-voltage operation is to ensure that power transistors operate in the Safe Operating Area (SOA) during current limitation. Thus, a bus voltage increase implies a reduction in trip-off time. Other consideration is the maximum blocking voltage and required derating for SiC JFET devices. In this regard, it should be noted that the proposed LCL would allow operation in the 300 to 400V range without major changes.

To verify the operation of the LCL at 300V, the prototype shown in Fig.4(b) has been used. For this purpose, the Z_1 bias source have been modified to operate at 300V. On the one hand, the Table II transistors Q_2 and Q_3 do not withstand the bus voltage and, on the other hand, the resistors R_3 and R_2 dissipate more power. Some transistors have been modified for packaging reasons, but those in Table II could have been used as well. The selected components and values are shown in Table III.

TABLE III:
LCL Class 3 @ 300V - Part List

Part	Ref	Part	Ref
J_1	UJN1205K	**Q_8**	DMMT5401
Z_1	10V	**Q_9**	DMMT5551
D_1	BAS521Q	**R_1**	255 kΩ
D_2	BAS521Q	**R_2**	10 kΩ
R_{shunt}	50mR	**R_3**	215 kΩ
M_1	SI4459ADY	**R_4**	10 Ω
D_{FW}	512-ES2D	**R_5**	100 kΩ
Z_1	10V	**R_6**	100 kΩ
Q_1	DMMT5551	**R_7**	500 kΩ
Q_2	FJV42	**R_8**	470 kΩ
Q_3	FMMT560	**R_9**	560 Ω
Q_4	BC807	**R_{10}**	30 kΩ
Q_5	2N2222A	**C_1**	1 µF
Q_6	DMMT5551	**C_2**	1 µF
Q_7	DMMT5401	**C_3**	63 nF

Fig.8 shows the response of the LCL tailored to operate at 300V, and I_{lim} = 2.8A. In this test a hard step load has been forced, starting from 470 Ω, as nominal load, to 5 Ω. Despite the I_{fault}=300V/5Ω=60A, the circuit reacts in less than 3μs and the maximum current is only 30 A. Although this is only a resistive load test and there is no energy stored in the load, it is worth noting that at the maximum stress condition, none of the components involved in current control exceed their operating limits. J_1 reaches 400 V and M_1 blocks 10 V, but additional tests are required using more complex loads (e.g. L-C filters).

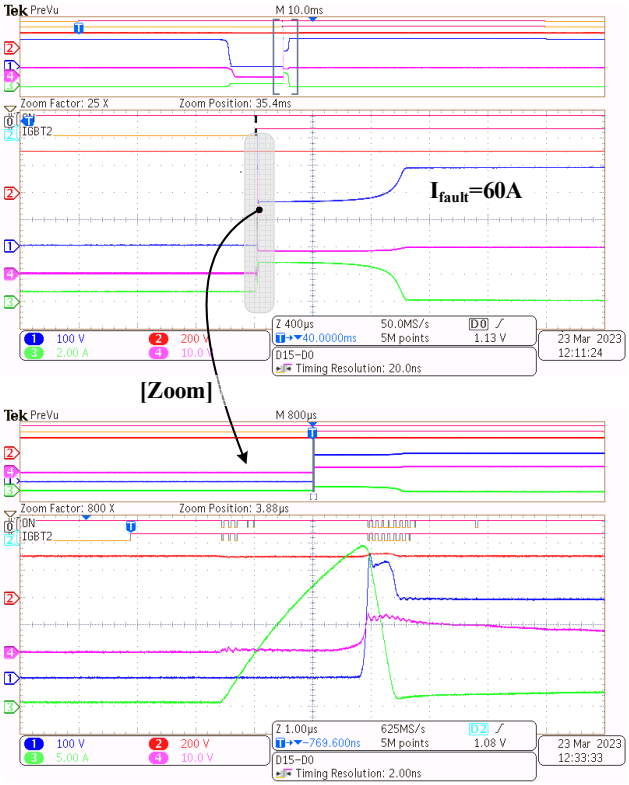

Fig 8. Class 3 – 300V LCL under hard load fault (5 Ω). In dark blue JFET V_{DS}, in red bus voltage, in green LCL current (M_1) and in magenta pMOS V_{SD}.

V. AGING AND ENDURANCE TEST CAMPAIGNS

In parallel to LCL design tasks, several test campaigns have been planned to increase the maturity of the proposed solution. Tests include power semiconductor tests and LCL tests. The first group are electrical characterizations at different stages of the test campaign (named functional tests in Fig. 9). The second group includes High Temperature Operation Life (HTOL) tests in nominal conduction operation, repetitive short circuit tests and repetitive inrush current tests. Single JFET configuration (LCL2A) and three paralleled JFET (LCL10A) configurations are being tested, using four different references of JFET transistors (T1 = UJN1205K, T2 = UJ3N065025K3S, T3 = UJ3N120035K3S, T4 = IJW120R100T1). TID and SEE tests are being planned.

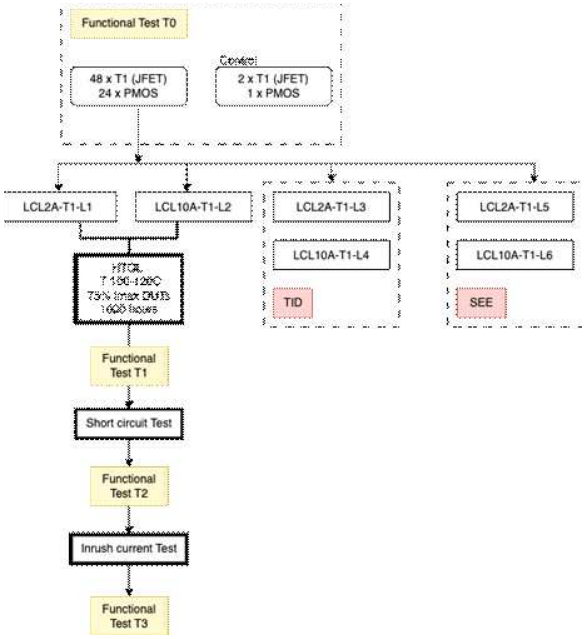

Fig 9. LCL aging and endurance test plan.

Initial characterization (Functional Test 0) has been completed using a B1505 power device analyzer from Keysight. As an example, the initial characterization of the JFET leakage current (I_{DSS} vs V_{DS}) and JFET input characteristics (I_D vs V_{GS}) are shown in Fig. 10 and 11, respectively, for reference UJ3N120035K3S.

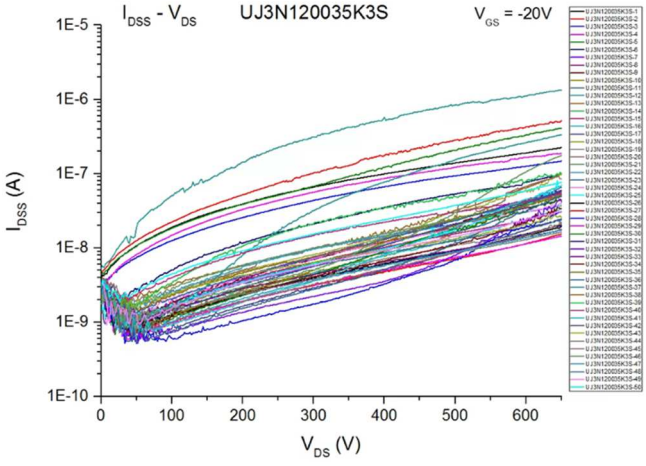

Fig 10. UJ3N120035K3S JFET initial leakage current (I_{DSS} vs V_{DS}) characterization (50 samples).

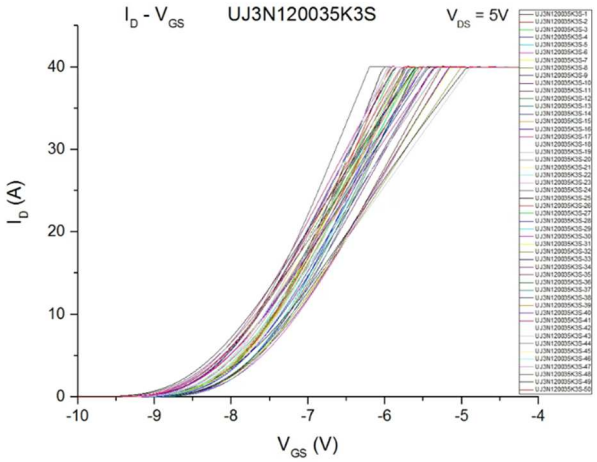

Fig 11. UJ3N120035K3S JFET input characteristics (I_D vs V_{GS}) characterization (50 samples).

The HTOL test, with 1000 h planned, consists of four LCL in series, for each part reference, operating at 75% of their maximum current rate with a controlled junction temperature of 100-110 ºC. Case temperature, V_{DS}, current and total voltage drop is monitored for LCL. Temperature control is performed in independent heatsinks with an axial-fan motor controlled by an industrial PLC. The block diagram of the HTOL test and a picture of the setup are shown in Fig.12 and Fig.13.

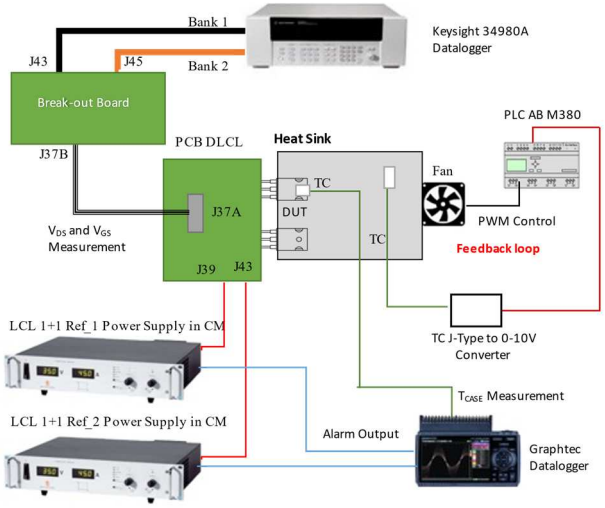

Fig 12. HTOL block diagram.

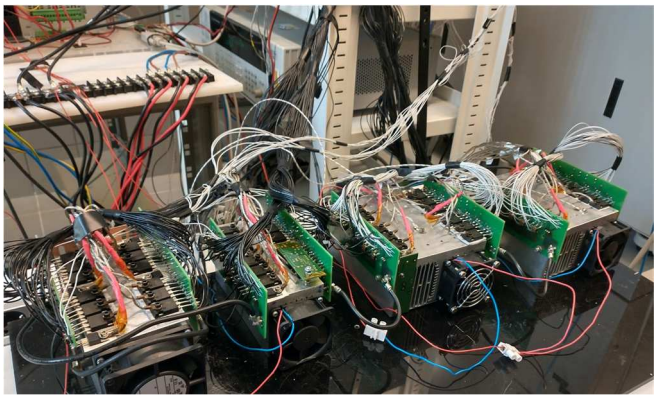

Fig 13. HTOL test setup photograph.

The HTOL is currently underway, so preliminary results of four LCLs (LCL13 – LCL16) are included as an example. Only pMOS and UJ3N120035K3S-JFET V_{DS} are shown in Fig.14 and Fig.15.

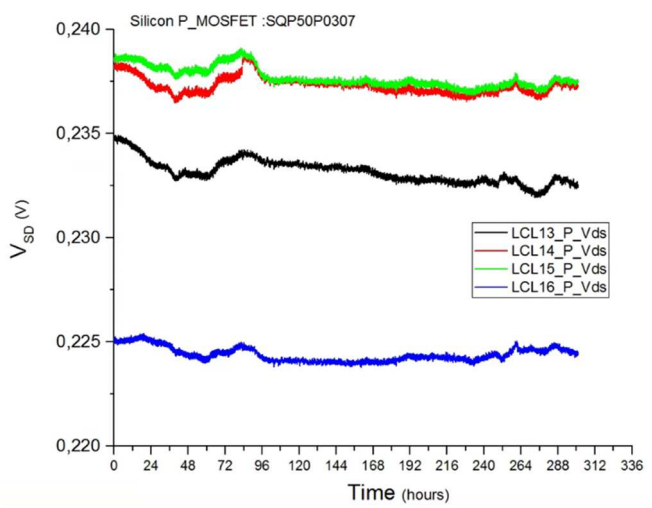

Fig 14. HTOL test: SQP50P03-07 pMOS-V_{DS}, 300 hours.

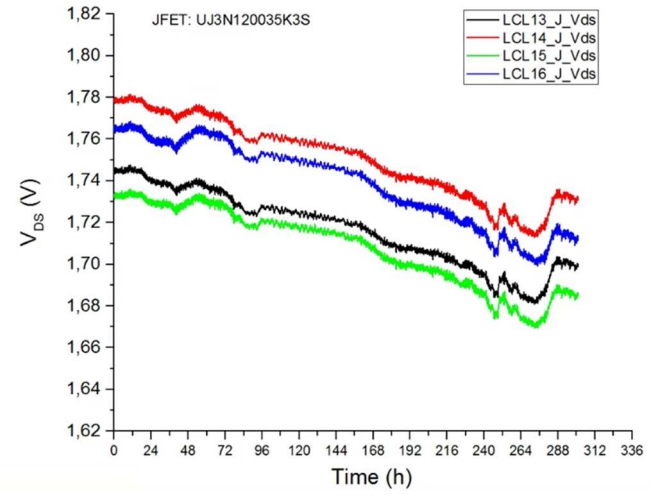

Fig 15. HTOL test: UJ3N120035K3S-JFET-V_{DS}, 300 hours.

VI. Conclusions

This work presents an alternative to high-current and high-voltage LCLs. The composite power switch, Si pMOS and SiC JFET in cascode configuration, combines the control advantages of pMOS transistors with the high-voltage and low on-resistance of SiC JFETs. The concept has been validated in 100V and 300V and an initial test campaign is started. Further studies, such as stability analysis or radiation hardness are still pending, being part of the next steps.

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